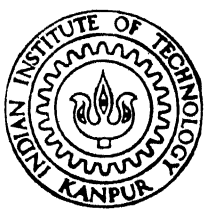
BIDIRECTIONAL POWER CONVERTER CONTROL AT UNITY POWER FACTOR OPERATION

By

RAMENDRA KUMAR TEWARI



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

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by

RAMENDRA KUMAR TEWARI

to the

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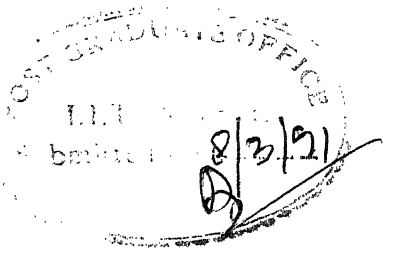

CERTIFICATE

It is certified that the present work entitled 'Bidirectoral power converter control at unity power factor operation' by ' Ramendra Kumar Tewari', has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

March, 1991.

(Dr. G. K. DUBEY)

Professor,

Department of Electrical Engg.

Indian Institute of Tech.

Kanpur.

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Finally, I express my regards to my parents for constant inspiration.

(RAMENDRA KUMAR TEWARI)

ABSTRACT

The present work involves the development of the expressions for unity power factor operation of the converter and then establishing the control requirements of the bidirectional power converters. A hardware control scheme has been developed for the bidirectional converter with unity power factor operation. The firing pulses for all the six switches of the bidirectional power converter are obtained for various load conditions. It is experimentally verified that the switching pattern corresponds to unity power factor operation.

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 GENERAL [2]

There are many industrial applications that require the conversion between AC and DC power and there are a number of methods by which this is currently performed. The Ward-Leonard motor-generator based system is among the oldest and is, in many respect, the ideal AC to DC power conversion method. It features sinusoidal input currents, good power factor, a variable DC output voltage and bidirectional power transfer. Ward-Leonard systems are still widely used because of these features, but are rapidly replaced by semiconductor based devices that offer lower purchase and maintenance costs and improved performance.

The 3-phase diode bridge is the simplest of a number of such devices. It offers high reliability, low complexity, and both good power-factor and voltages regulation. Unfortunately, the output voltage of the device cannot be controlled and because of the unidirectional nature, power transfer can occur only from AC side to DC side. Furthermore, the input currents are non-sinusoidal which is of growing concern to electricity supply authorities as the harmonic content of such waveforms can cause numerous problems within the power system.

1.2 LINE COMMUTATED THYRISTOR CONVERTER [1]

The AC to DC line Commutated converters are employed in

(a) DC drives

(b) As a front end converter in VSI and current source inverter fed induction and synchronous motor drives

(c) Slip power recovery control of induction motor

(d) As a basic building block of cycloconverter

(e) HVDC transmission, etc.

The line commutated thyristor converters used in these applications suffer from three common drawbacks :

(i) They produce low frequency harmonics at source terminals

(ii) Operate at low power factor for large firing angles

(iii) Their output voltage consists of ripple or low frequency harmonics.

The harmonics generated at the source terminals have a number of undesirable effects such as malfunction of electronic equipment connected to the line, excitation of system resonances, overloading of capacitors, decrease in efficiency owing to increase in losses due to harmonic currents and skin effect, interference, with telephone lines and saturation of transformers. The reactive power drawn from the line, when operating at low power factor, increases transmission losses, and maximum power demand, and has adverse effect on voltage regulation and supply system stability. Because of their wide applications, the converter load now forms a significant proportion of the total load on the utility. With the replacement of conventional drives with semiconductor controlled drives, their share of load on utilities is likely to grow. Therefore, it is a matter of great concern today to alleviate these problems.

The harmonic content decreases and the frequency of dominant harmonics increases as the converter pulse number is increased. The high frequency harmonics can be filtered out by small inexpensive filters. 12, 24 pulse converters are economically viable only at high power levels. At low power levels only 6-pulse and 2-pulse converters are used. In case of electric traction, even at high power levels, only single phase supply is used, consequently 2-pulse converters can only be employed. The traction supply system is usually weak in nature. Therefore, the harmonics and reactive power pollute the supply to a greater extent.

The low frequency harmonics in the output voltage deteriorate the performance of the load. In case of DC drive fed by line commutated thyristor converters, these harmonics produce a ripple in the armature current. The ripple causes derating of the motor because of the increase in loss and reduction in machine's current commutation capability. The ripples are also responsible for causing discontinuous conduction which increases speed regulation and slows down the transient response of the drive. When used in a closed loop system, with a linear controller, the transient response becomes sluggish, making it necessary to use more sophisticated controllers. The magnitude of ripple and region of discontinuous conduction increase with the decrease in converter pulse number.

The methods, employing line commutation, used for having an improved power factor are controlled flywheeling in fully controlled converters, sequence control, bias voltage control. In single phase fully controlled converters, the controlled flywheeling yields the

performance similar to the half controlled converter, while retaining inversion capability. Again during inverter operation it gives a performance superior to that with conventional operation. The sequence control of series connected single phase converters has been used in traction, employing two stages and higher stages. The performance of fully controlled converter in sequence control is further improved when controlled flywheeling is also used. A single stage fully controlled converter with controlled flywheeling yields the same performance as two stage converter operating with conventional operation, thus, allows substantial saving in the cost of devices and transformer.

1.3 PWM CONVERTER [4]

The pulse width modulation (PWM) converter is a potential challenge to the venerable thyristor Graetz bridge at the rectifier end of the variable speed AC drive system.

The merits of current controlled PWM power modulator are :

(1) It delivers near sinusoidal currents, thus obviating expensive low frequency harmonic filters.

(2) It is capable of unity and even leading power factor operation, thus, offering the option of the power factor compensation.

(3) It has bidirectional power flow capability as compared to the need of dual converters of the Graetz bridge configuration.

Important PWM techniques are: single pulse modulation, equal PWM, sinusoidal PWM, selective harmonic elimination and current controlled PWM.

Both the single converter and more than one converter in sequence control, the sinusoidal PWM highest power factor and least harmonics content in the source current, and therefore, gives the best performance on the source side. The equal PWM has the least ripple on DC side. The selective harmonic elimination method is suitable where certain undesirable harmonics should be reduced to practically zero. For example, in traction it is necessary that the converter does not produce harmonics having frequency of track circuits employed for the operation of signals.

1.4 BIDRECTIONAL POWER CONVERTER

For four quadrant operation of voltage source inverter fed AC drives with regenerative braking, a two quadrant converter capable of operating in quadrants one and two (variable voltage in one direction and current in either direction) is sufficient. Because of the non-availability of a suitable two quadrant converter, a dual converter has to be used. Since such a converter becomes very expensive, the regenerative braking is used only in limited cases of large power.

Similarly there are a number of DC drive applications where speed reversal is not required, but regenerative braking is required. Here also a two quadrant converter capable of operating in quadrant one and two is required. However, due to non-availability of a suitable two quadrant converter, a dual converter (4-quadrant converter) is used.

In the recent years the capability of voltage source inverter to work as a 2 quadrant converter (I & II) has been explored.

Because of the above mentioned problems of dual converter and other conversion schemes, considerable interest has been developed in this feature of voltage source inverter.

The control strategy of this VSI is different when it is to be used as a bidirectional power converter. Also with proper control scheme it is possible to operate the bidirectional power converter at unity power factor at AC source end. The source current can be made to even lead the voltage if reactive power compensation is required.

The present work involves the development of the expressions for unity power factor operation of the converter and then establishing the control requirement of the bidirectional power converters. A hardware control scheme has been developed for the bidirectional converter with unity power factor operation.

Because of low switching speeds of thyristors and forced commutation problems thyristors are not used in bidirectional power converter. The GTO is now available upto 3000 A, 4500 V; power transistor upto 1000 V, 60 A; MOSFETs upto 1000 V, 50 A. The use of MOSFETs in this application has been studied and protection circuits for MOSFET converters are studied.

However, due to non-availability of MOSFET's proper rating, the control scheme could not be tested on a power module. But, the firing pulses for all the six switches of the bidirectional power converter are obtained for various load conditions. It is experimentally verified that the switching pattern corresponds to unity power factor operation.

CHAPTER 2

LITERATURE REVIEW OF BIDIRECTIONAL CONVERTER AND ITS CONTROL

References 2,4,5,6,14,15 describe the bidirectional converters. Papers (14,15) describe a novel AC/DC converter which incorporate a number of features such as unity power factor, sinusoidal input currents and regeneration capability. They use pulse width modulation (PWM) techniques to achieve these features and are essentially current sourced converters as the DC output is a controlled current as opposed to the voltage. The problem with such a current source converters is that they should be driven by a current source. Thus considerable filtering on the AC side is required to prevent high frequency harmonics present in input currents from entering the power system. Also in many applications the DC side voltage should be constant rather than DC side current.

Reference 2 describes a reversible voltage sourced rectifier, i.e. voltage source bidirectional converter while papers (4,5,6) describe the indirect current controlled bidirectional power converter.

2.1 INDIRECT CURRENT CONTROLLED THREE PHASE RECTIFIER [4,5,6]

Figure 2.1 shows the block diagram of rectifier inverter link. The rectifier and the inverter are identical controlled current PWM modulators. The hysteresis band control confers to the modulator the controlled current feature. This is accomplished by applying ON/OFF switchings of the bipolar transistors so that the current in each phase tracks the reference current waveform within a narrow tolerance band.

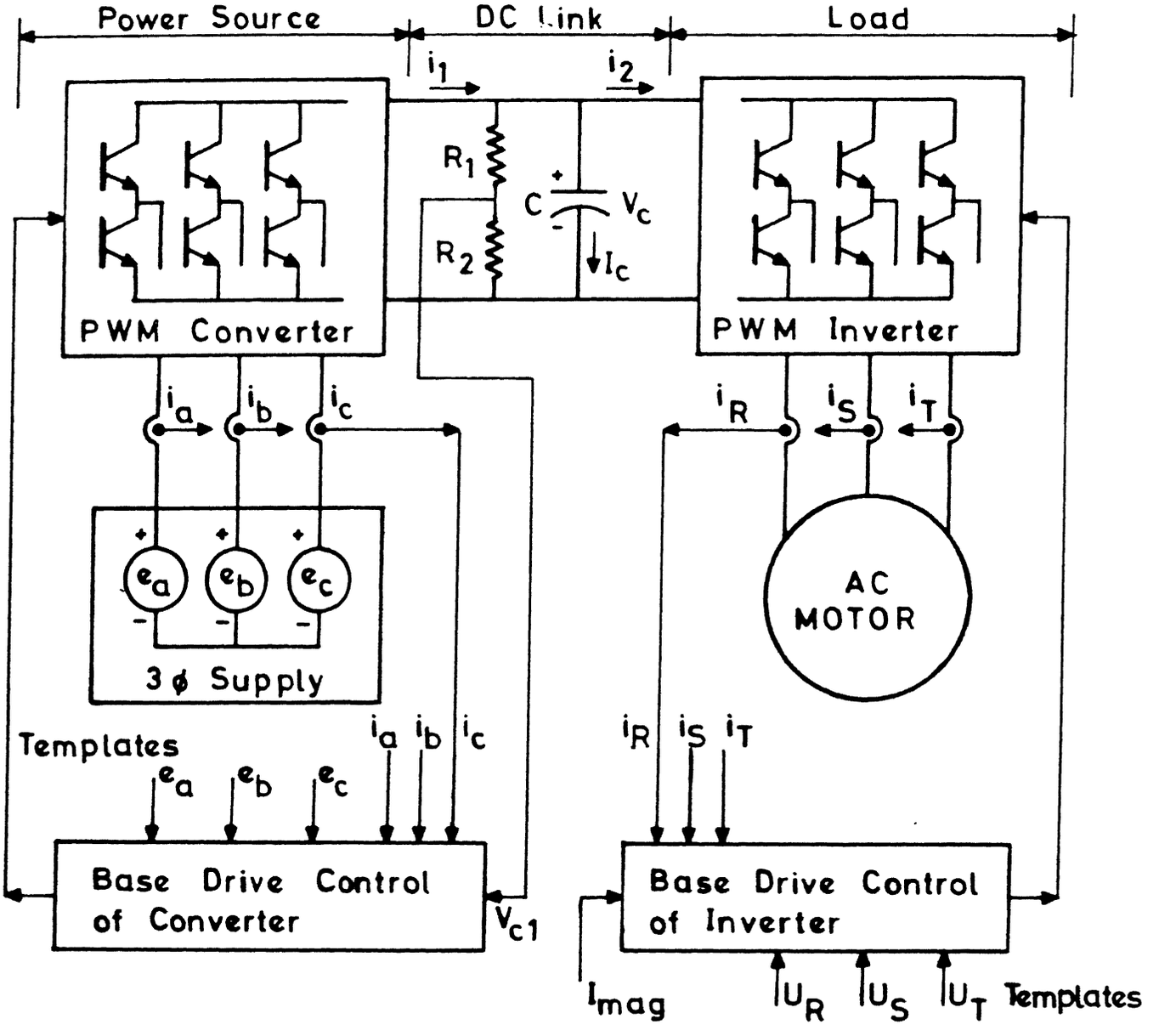


Fig. 2.1 Schematic of controlled current PWM rectifier/ inverter A.C. drive.

The operation of PWM current controlled inverter is well established. The review therefore will mainly concentrate on controlled current PWM converter. In the modulator, reference voltages are taken by voltage transformer from phase voltages. Phase shifting is introduced for power factor correction. Some electronic filtering may be required to filter third harmonic due to transformer saturation. As in case of inverter, the phase currents are made to track the tempelate waveforms within a narrow tolerance band of width 'h' by a hysteresis control in the Base Drive Control circuit.

2.1.1 DC Link

The two PWM modulators are connected as shown in Figure 2.1. The shunt capacitor 'C' serves two functions:

1. Filters ripple in DC link voltage
2. Stores charge to maintain a sizeable DC link voltage V_c.

2.1.2 Operating Characteristics of Current Controlled PWM Modulators

Previous work [16] has identified that there are two limits, which have been given the names 'loss of control limit' and 'current waveform distortion limit'.

The second design consideration is one of ensuring that the current control of the inverter and the current control of the rectifier be coordinated so that the power demanded by a.c. motor is matched by the power supplied by a.c. voltage source. The command which signals a reversal of power flow in the inverter must also simultaneously signal a reversal of power in the rectifier.

2.1.2(A) Loss of Control Limit

It is relevant in the rectifier operation only. A cursory glance over Figure 2.2 will draw attention to the fact that the 6 free-wheeling diodes across transistor T_1 ... T_6 for a diode bridge, which can rectify power from AC voltage source. A basic requirement of the PWM rectifier operation is that the voltage V_c across the DC link is always high enough so as to reverse bias all these diodes. In reference [16] it is established that the PWM looses control when,

$$V_c < \frac{3\sqrt{6}}{\pi} V_m \qquad (2.1)$$

where V_m is the rms phase AC voltage measured at the modulators terminals.

2.1.2(B) Current Distortion Limit

When the AC phase voltage at the modulator terminals V_m has a magnitude that exceeds the DC link voltage V_c in the inequality

$$V_c < \sqrt{6}\ V_m \qquad (2.2)$$

There is insufficient resultant voltage to force the current through the inductances so as to track the desired template waveforms. Equation (2.2) has been derived analytically, although no proofs have been published. Reference [16] has given experimental results which substantiate Equation (2.2).

2.1.3 Power Matching in Modulators

Using the symbols V_m, I, ϕ, respectively to denote the rms value of the phase voltage at the AC terminals of the modulator, the phase current and the power angle, and using suffix r and i for quantities in the rectifier and inverter side, the static power continuity of the DC link (neglecting modulator losses) is

$$3\,|V_{mr}||I_r|\cos\phi_r \;=\; 3|V_{mi}||I_i|\cos\phi_i \qquad (2.3)$$

On the rectifier side, ϕ_r, is set by the phase shift control. When the rectifier AC side resistances and inductances are small V_{mr} is approximately, the voltage of the AC supply. The controllable parameter is $|I_r|$, which is controlled by I_m, (Figure 2.1) where

$$|I_r| \;= I_m/\sqrt{2} \qquad (2.4)$$

On the inverter side the phase current magnitude $|I_i|$ is controlled by I_{mag} (Figure 2.1) where

$$|I_i| = I_{mag}/\sqrt{2} \qquad (2.5)$$

2.2 VOLTAGE SOURCED REVERSIBLE RECTIFIER [2]

Figure 2.2 shows a voltage sourced bidirectional converter capable of working as rectifier and inverter both.

The difference between the converter of Figure 2.2 and a conventional 3 phase rectifier bridge is the presence of 6 self commutating switches 1 to 6. After the output capacitor has charged the $\sqrt{6}\,V_s$ via the diode bridge, the diodes get reversed biased. Turning one of the self commutating switch in each of the three legs will cause currents to flow in the inductors and capacitor because of a potential difference across the inductors. Because of the inductive nature of AC side, when a conducting self commutating switch is turned off, the current through the inductor free wheels through the diode, on the opposite side of the leg. If a control scheme is used in which whenever a switch is turned on, the switch in the opposite leg is turned off, then this free-wheeling action does not compromise the operation in any way because the current happens

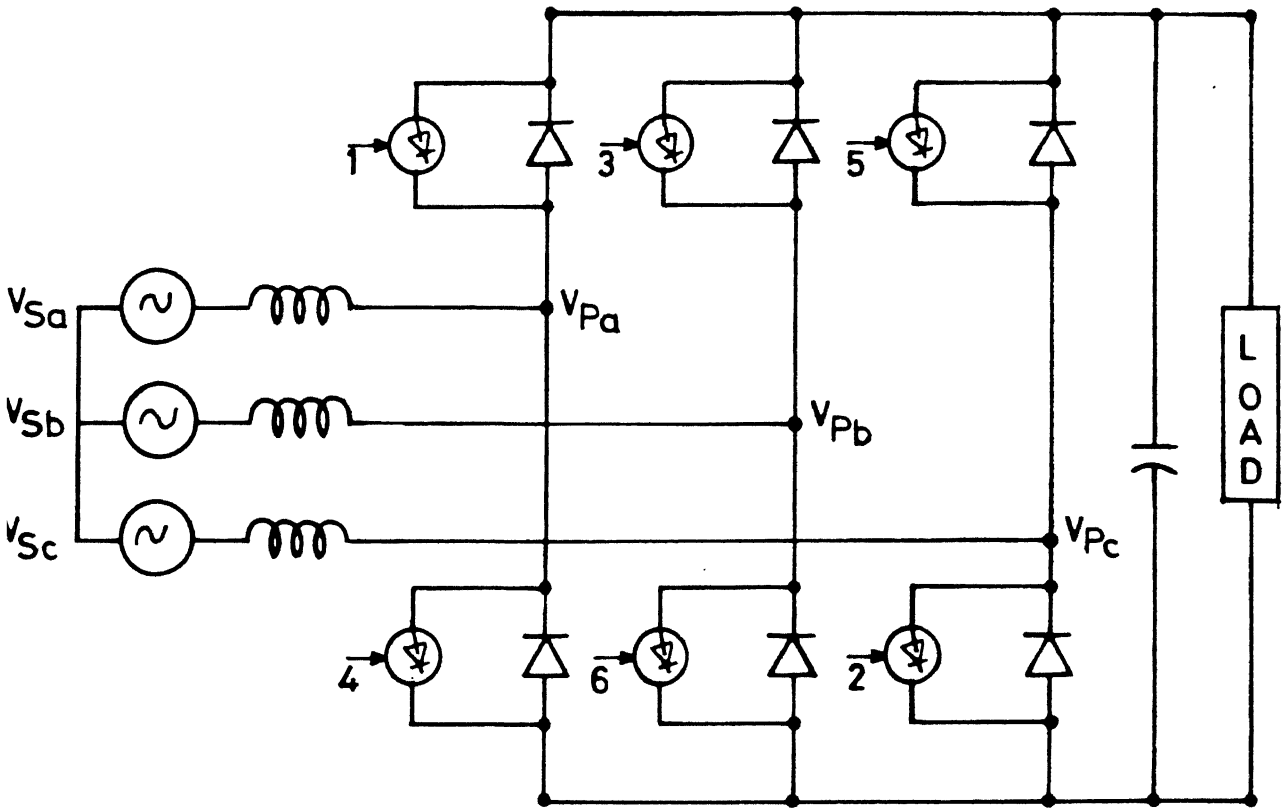


Fig. 2.2 Voltage sourced bidirectional converter.

to be flowing in a diode or a transistor is irrelevant. By appropriately connecting the inductors between the positive and negative buses, the current can be made nearly sinusoidal. Further the magnitude and phase of line currents can be controlled and hence the power transfer that occurs between the AC and DC sides can be controlled.

The operation of the voltage source inverter as a bidirectional converter can be viewed from another angle also. Considering a voltage source inverter, fed induction motor drive, when induction motor regenerates the power from the induction motor, which can be assumed to be a three phase AC source behind a inductor in every phase, is fed to the DC side. By using an appropriate inductor in every phase of AC lines, it can be treated as equivalent induction motor and the power from the source (AC mains which can be assumed to be a regenerating induction motor) can be fed to the DC side as well.

The operation and performance of this type of converter is discussed in detail in Chapter 3.

2.3 USE OF MOSFETs IN BUILDING BIDRECTIONAL POWER CONVERTER

Power MOSFETs are now being used in power electronics in the Kilo-Watt range. One of the attractive feature of the MOSFET is the integral diode in anti-parallel, which can be used as free wheeling diode in many systems.

Power MOSFETs are frequently used in place of bipolar transistors in low and medium power applications owing to its following features :

- faster switching speed
- simple gate drive
- forward-bias safe operating area for the MOSFET is large
- as a majority carrier device, it has a positive temperature coefficient of on-resistance which prevents thermal instability or hot spots.

The excellent switchings capabilities of Power MOSFETs make possible the construction of PWM inverter operating at high switchings frequency.

Due to the limited current carrying capacity of MOSFET suitable for line voltages the parallel operation becomes a must. Thermal degeneration property makes power MOSFETs useful for parallel operations. This property helps power MOSFETs in avoiding current in balance between individual devices (no resistors required). Current shared between the parallel MOSFETs is sensitive to the source circuit and the impedance of the device.

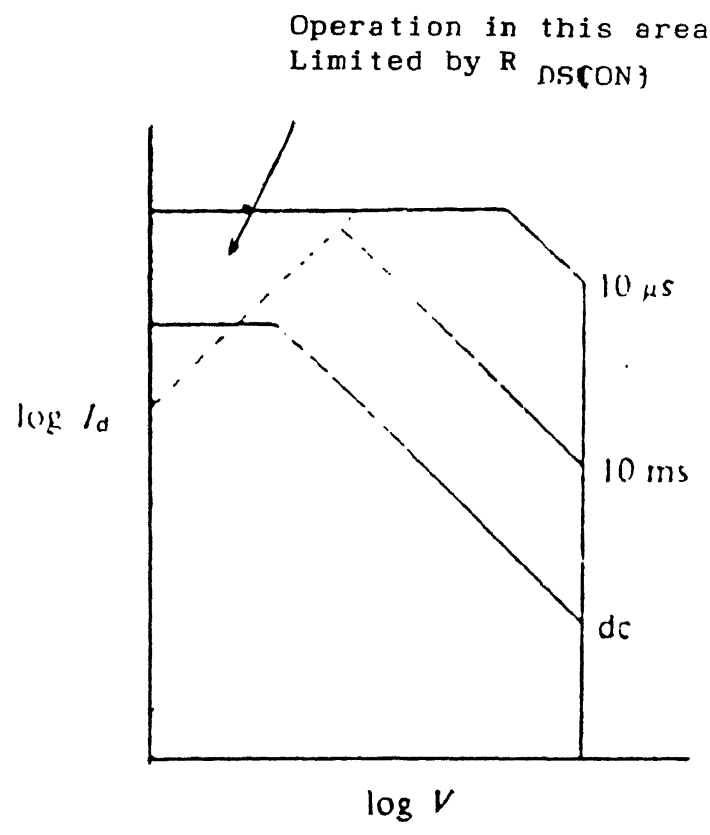
2.3.1 Comparison of MOSFETs and BIPOLAR Transistors

(a) Conduction mechanism

In power MOSFETs majority carriers alone are responsible for current flow, whereas in bipolar transistors it is regulated by minority carrier injection.

(b) Electron concentration

In power MOSFETs, electrons and holes are separated by dielectric. So no recombination is possible and gate current only flows when charge is being established or removed; while in bipolar transistors recombination takes place between the electrons and the holes and it becomes necessary to inject base current continuously in order to maintain the required hole concentration.



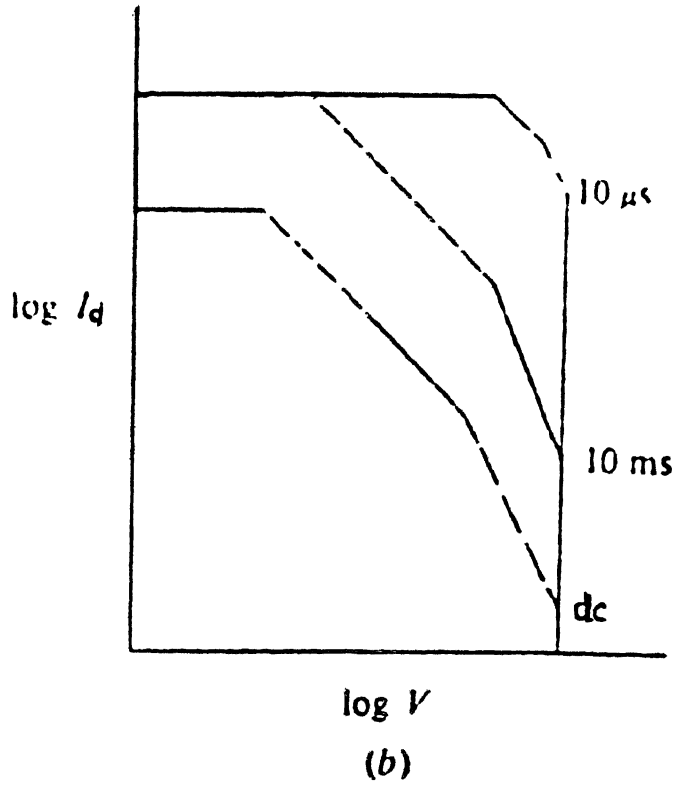


FIGURE 2.3: Safe-operating-area curves.
(a) MOSFET; (b) Bipolar transistor.

(c) Drive requirement

Power MOSFETs require application or removal of a relatively small amount of charge at turn on and turn off of the device as compared to the bipolar transistors.

2.3.2 Appropriate Application

Performance and cost are the two main issues on which the choice between a MOSFET and a bipolar transistor is usually made.

In terms of performance the MOSFET has following advantages :

- low switching losses
- low gate drive requirements
- freedom from second breakdown.

The voltage drop across a high voltage MOSFET is usually greater than that across bipolar transistor of the same size, because the voltage drop across is bipolar transistor depends less on the voltage rating.

2.4 POWER MOSFET FAILURE DURING TURN OFF [9]

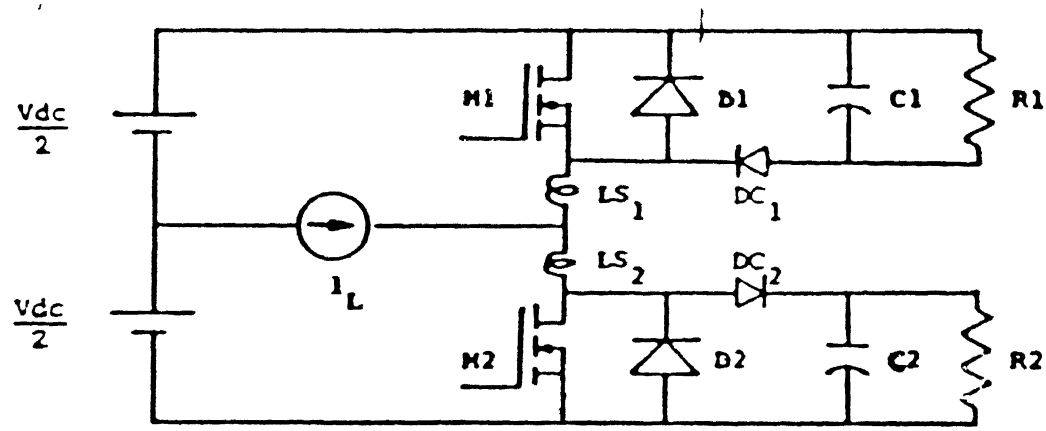
The Power MOSFET is frequently used in place of bipolar transistors because of its faster switching speed and relatively simple gate drive requirements. Also, the forward bias safe operating area for the MOSFET is larger as compared to bipolar transistor, because the MOSFET as a majority carrier device, has a positive temperature coefficient of ON resistance. Thus, Power MOSFET does not experience thermal instability. Thermal instability and hot spots lead to second break down (or snap back) and greatly limit the forward bias safe operating area of bipolar transistor.

The turn-off safe operating limits of the power MOSFET are limited by second breakdown. The activation of the parasitic bipolar transistor during turn off is responsible for the second breakdown failures. The applications that place the greatest stress upon the MOSFET require fast switching with inductive drain loads. It has been suggested that very large values of dv/dt (and related capacitive dv/dt current) may cause the parasitic bipolar transistor to become active and cause the Power MOSFET to fail. Recent works show, in commercially available devices, second breakdown failure of the MOSFET is initiated by Avalanche current, which activates the parasitic bipolar transistor. Capacitive dv/dt, in commercial devices, are not sufficient to cause second breakdown during normal switching.

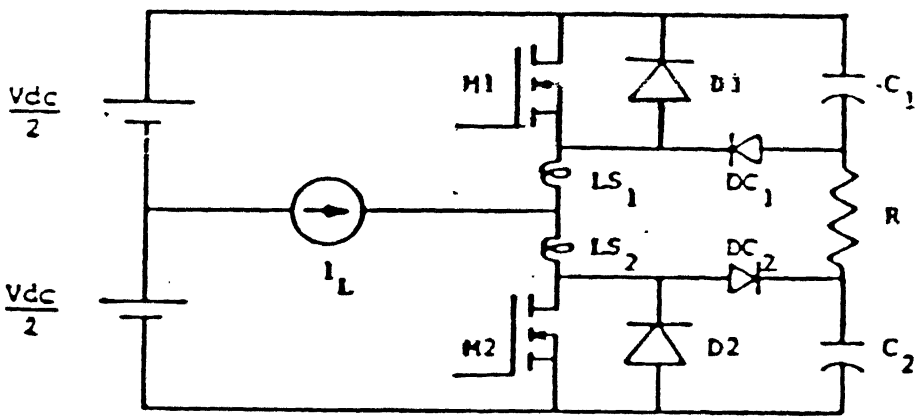
The electrical state of the intrinsic drain-source diode immediately prior to switching has a significant effect on the turn off failure. If the diode was forward bias just prior to the sudden application of drain voltage, the parasitic bipolar transistor is much more susceptible to turn on (and thus causes the Power MOSFET to fail).

2.5 VOLTAGE CLAMP CIRCUITS FOR A POWER MOSFET PWM CONVERTER [10]

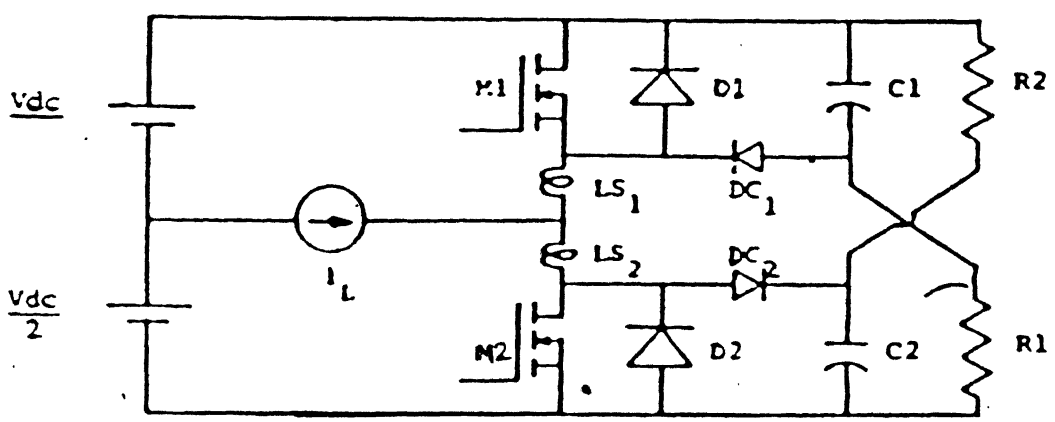
The Power MOSFETS can carry instantaneous or pulse currents upto four times the rated capacity, but any significant increase in voltage over the rated value damages the device permanently. Further, the ability of Power MOSFETs to carry current is essentially limited only by the junction heating, both for switched and linear modes of operation - unlike the bipolar transistor which is limited



(a) Clamp 1



(b) Clamp 2



(c) Clamp 3

FIGURE 2.4: Voltage Clamp Circuits.

by its gain and the second breakdown. In other words, Power MOSFETs can switch at high voltages and currents safely and no current snubbing circuitry is essential. Hence, for a Power MOSFET, the snubber circuit essentially reduces to a voltage clamp circuit, in order to keep the voltage spikes at switch off within the specified limits.

2.5.1 Analysis of Clamp Circuits

In this section, three types of voltage clamp circuits which can be used with Power MOSFET in the bridge (or totem pole) circuit configurations are considered. Detailed analysis of clamp circuit III is outlined in Section 2.5.1(A).

2.5.1(A) Voltage Clamp Circuit III

In this circuit the discharge resistors R_1 and R_2 are connected in series with C_1 and C_2 as shown in Figure 2.4(c). Since C_1R_1 and C_2R_2 series combinations are connected across positive and negative buses so the voltage across C_1 and C_2 can not fall below V_{dc} at any instant of time.

Switching waveforms for one complete cycle of operation is shown in Figure 2.5.

Considering the state when MOSFET 1 is conducting. It is represented by t=0 instant of Figure 2.5. The load current path is through supply ($V_{dc}/2$) - MOSFET1 - LS_1 - LOAD - ($V_{dc}/2$). The inductor LS_1 current $i_{L1} = I_L$.

At $t = t_a$, M_1 is turned off by removing its gate drive. The load current I_L flowing through inductor LS_1 (i_{L1}) cannot at once reduce to zero so it takes a path through C_1 and diode DC_1 as shown

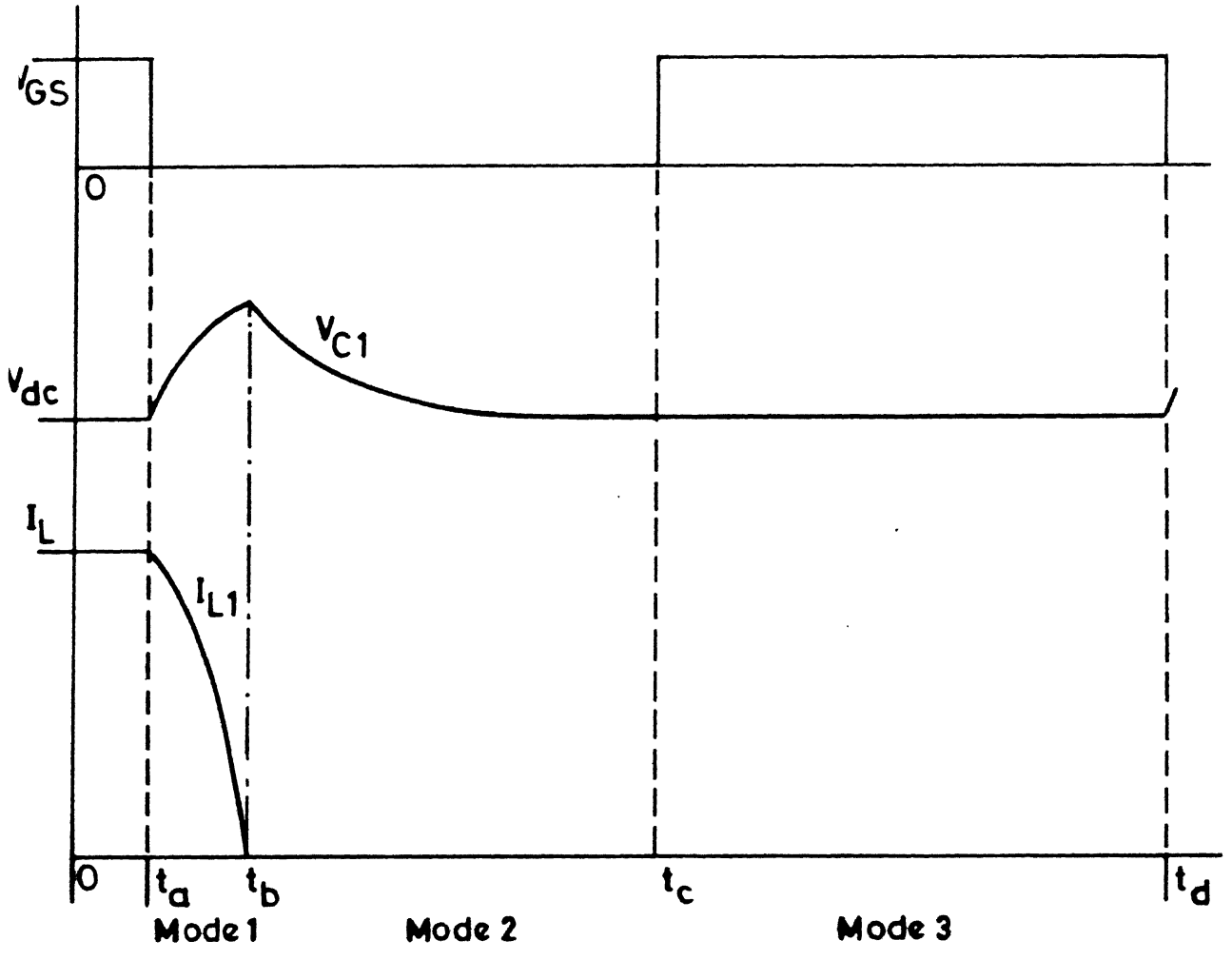


Fig.2.5 Voltage and currents waveforms in clamp circuit 3.

in Figure 2.6. This current flowing through clamp capacitor C_1 tries to overcharge it. Any increase in capacitor voltage V_{c1} forward biases diode D_2 which starts conducting and sharing the load current.

The circuit now appears as a series LC circuit with capacitor C_1 in series with LS_1 and LS_2 having an initial current equal to I_L. The equation of current flowing through LS_1 for this period is given by Eqn.(2.6)

$$i_{L1} = I_L \cos \omega t \tag{2.6}$$

where, $\omega = C_1 (LS_1 + LS_2)$

$=$ ringing frequency in radian per second.

The equation of current through inductor LS_2 (i_{L2}) is given by Eqn.(2.6A).

$$i_{L2} = i_L - i_{L1}$$

$$= I_L - I_L \cos \omega t \tag{2.6A}$$

From Eqn.(2.6) and (2.6A) it is clear that current i_{L1} is reducing and i_{L2} is increasing. At time instant $t=t_b$, the current i_{L1} falls to zero and diode DC_1 goes off. At this instant current through LS_2 i.e. i_{L2} reaches load current I_L.

The overcharging of capacitor stops with current i_{L1} falling to zero. The peak capacitor voltage occurs at instant t_b which is given by Eqn.(2.7)

$$V_{c1\ max} = V_{dc} + 2\omega L\ I_L \tag{2.7}$$

where, $L = LS_1 = LS_2$

The capacitor now discharges to V_{dc} during period $t_c > t > t_b$ (represented by MODE2) through R_1C_1 combination as shown in Figure 2.7.

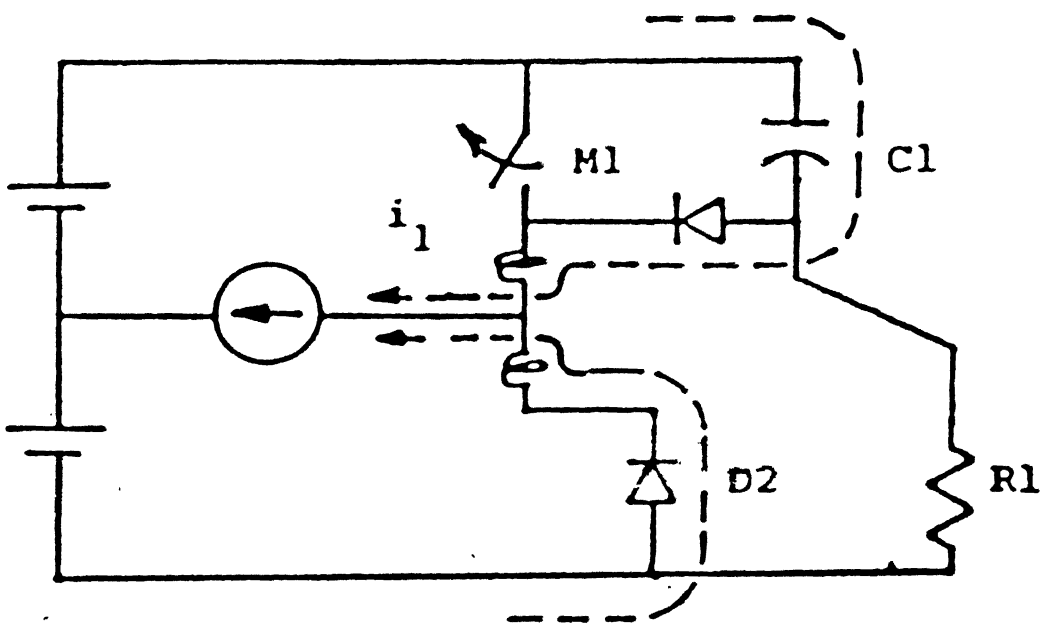


FIGURE 2.6 : Mode 1 of operation of clamp circuit 3.

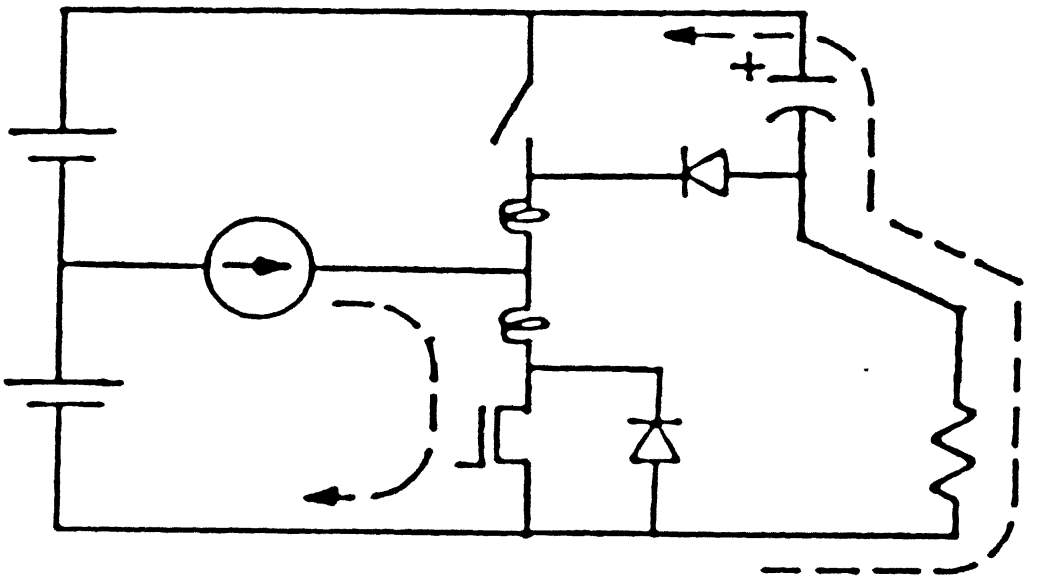


FIGURE 2.7: Mode 2 of operation of clamp circuit 3.

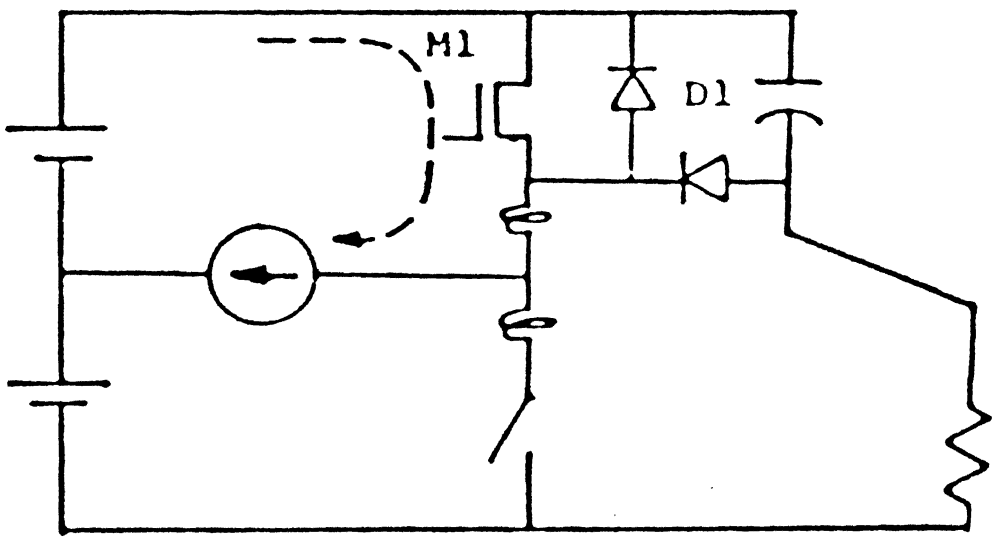


FIGURE 2.8: Mode 3 of operation of clamp circuit 3

At $t=t_c$ gate pulse is again applied to MOSFET M_1 so it starts sharing load current I_L. It is shown in Figure 2.8

Various modes of operation defined in Figure 2.5 are :

Mode 1 $t_a < t < t_b$ capacitor overcharge period

Mode 2 $t_b < t < t_c$ capacitor discharges to V_{dc}

Mode 3 $t_c < t < t_d$ Load transferred back to MOSFET M1.

This type of clamp circuit has some important advantages compared to the two types mentioned previously. Since the capacitor is connected across the DC bus through a series resistance, the change in the voltage across the capacitor during any switching cycle is only $V_{dc}+2.\omega.L.I_L-V_{dc} = 2.\omega.L.I_L$, compared to $V_{dc}+2.\omega.L.I_L-V_c(o)$ in other types. This leads to considerable decrease in the clamp circuit power loss during switching operations. The resistance can be small in this type of clamp circuit which will decrease the capacitor discharge time during mode-3. A small value of R also decreases the peak voltage on the capacitor, because when C_1 charges beyond the supply voltage during Mode-1, it also discharges through the source and R_1. If R_1 is small this discharge cannot be neglected.

2.6 DESIGN OF CLAMP CIRCUIT COMPONENTS

2.6.1 Design of Clamp Circuit Capacitor

Let 'X' p.u. be the permissible overshoot. Knowing 'L', the stray inductance in the circuit, the value of clamp capacitance to be used to keep the overshoot within limits is determined by using the following equation :

$$C = 2.L.\ [I_L/(X.V_{dc})]^2 \qquad (2.8)$$

where $X = [V_{c(max)} - V_{dc}]/V_{dc}$.

2.6.2 Design of Clamp Circuit Discharge Resistor

The value of R for clamp-1 can be determined as,

$$R \leq [\ T/2\ .Z_1.C] \tag{2.9}$$

The value of R_1 for clamp circuits 2 and 3 is given by

$$R \leq [\ T/2.Z_2.C\ ] \tag{2.10}$$

For clamp 3, the value of resistance can be lower than that given by Eqn.(2.10) and still the clamp circuit power loss will remain unaffected.

2.7 ISOLATED GATE DRIVE CIRCUIT FOR INVERTER APPLICATION

The gate driver must meet the following requirements :

- short delay time
- low impedance output
- capability of accepting duty cycles between 0% and 100%
- insusceptibility to dv/dt triggering during switching
- low capacitance between the two side of the power supply.

A suitable arrangement is shown in Figure 2.9. Isolation is provided by 2601 optical coupler. This has a Faraday screen between the LED and photo transistor to prevent spurious triggering of phototransitor by capacitive currents during switching of the power circuit.

Gate drive is provided by a MOSFETs driver 1C, which is capable of providing 6A of charging current and it is wound on independent bobbins with air gap separation of the two windings to reduce capacitive coupling between them.

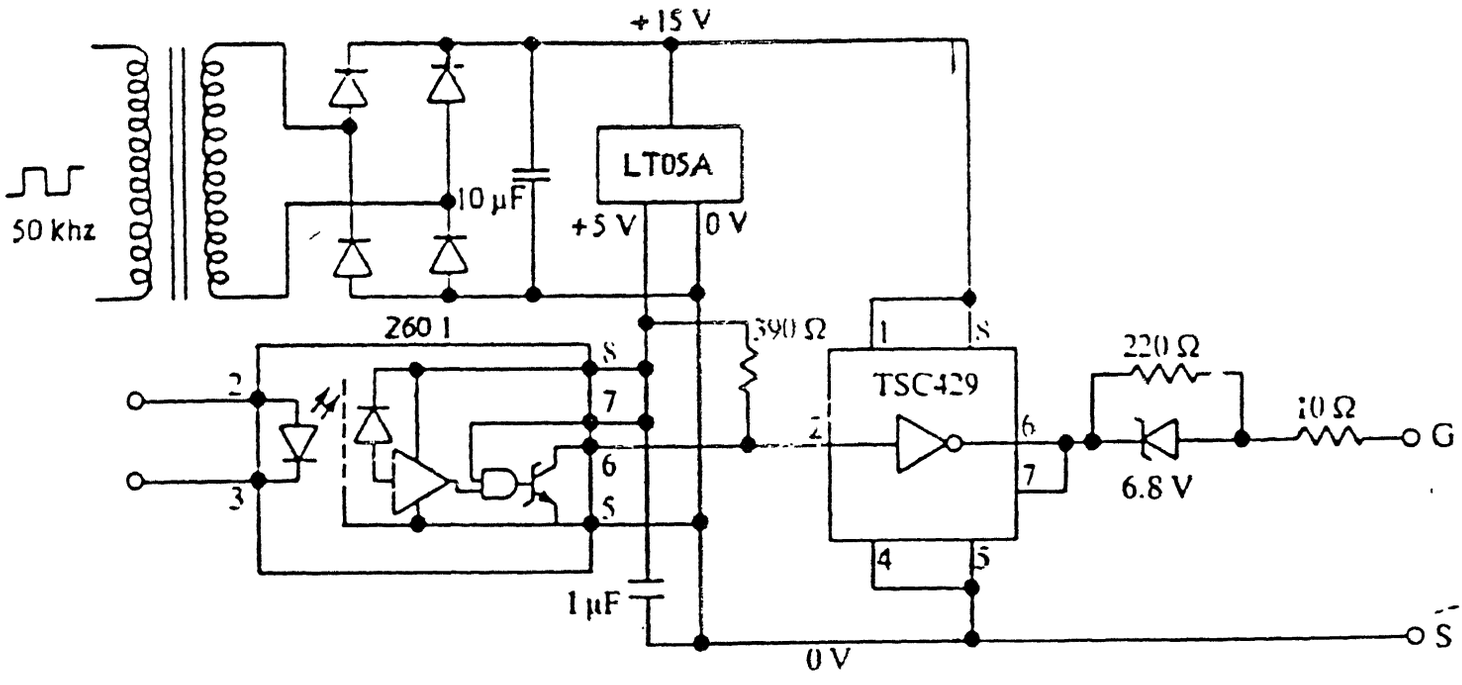


FIGURE 2.9 : Isolated gate drive circuit for inverter applications.

CHAPTER 3

CONTROL REQUIREMENT OF BIDIRECTIONAL POWER CONVERTER

The power circuit of a bidirectional converter resembles to that of a voltage source inverter. Operation of this converter as an inverter is well established and control schemes have been suggested for its operation and control. The use of this converter in rectification has been reported only recently.

3.1 PRINCIPLE OF OPERATION OF A BIDIRECTIONAL CONVERTER

A bidrectional power converter consisting of 6 diodes and 6 self commutating switches is shown in Figure 2.2. As mentioned earlier, if we do not consider six self commutating switches for a moment then the converter is nothing but a simple 3 phase bridge rectifier. Once the output capacitor C_o gets charged to a voltage $\sqrt{6}V_s$ the diodes get reverse biased.

Now looking at the converter as a voltage source inverter, the desired sinusoidal current wave forms on the AC side can be produced if the six self commutating switches are controlled in a sinusoidal PWM manner to produce three phase PWM voltages V_{pa}, V_{pb} and V_{pc} at the mid point of the three legs as shown in Figure 2.2. The PWM voltages produce harmonics as multiples of the switching frequency.

The impedance of the inductor and the magnitude and phase of V_p, with respect to the main supply, determines the fundamental component of current that flows through the inductor. Additional voltage harmonics do produce similar line current harmonics but their magnitude is drastically reduced because of the presence of the

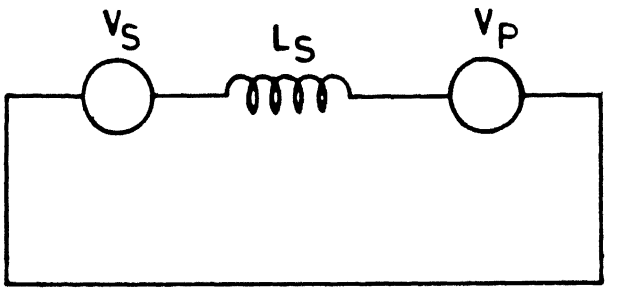
inductors which offer an increasingly higher impedance as the harmonic order increases. Tripplen harmonics are absent. By using asymmetrically sampled sinusoidal PWM and by making the switching frequency an odd multiple of three of the supply frequency, even harmonics can be eliminated.

3.2 OPERATION

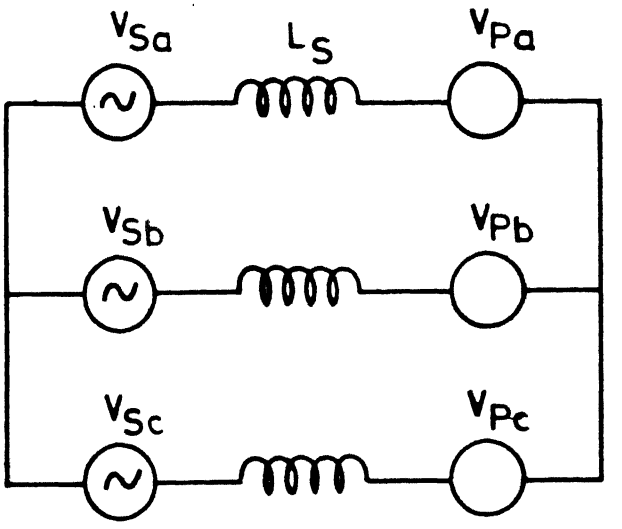
The operation of the bidirectional power converter is analogous to that of a 3-phase synchronous machine. As explained in Section 3.1, the switches are operated to produce balanced 3-phase fundamental voltages. Under this condition the system shown in Figure 2.2 can be represented by a simple equivalent circuit of Figure 3.1.

Therefore, as with the simplest model of a synchronous machine, consisting of three inductors with AC voltages imposed at either end, the magnitude and direction of power flow is dependent on the magnitude and the phase of the two voltages and the size of the inductor. At unity power factor, the phasor diagram showing source voltage V_s, synthesised PWM voltage V_p and drop across inductor V_L is shown in Figure 3.2.

If V_s leads V_p, then the power transfer is from source V_s to the source V_p and vice versa. The reactive power flow from V_s can be made equal to zero by adjusting the magnitude of V_p so that the current lags the voltage V_L across the inductor by 90° and flows in phase with V_s. Thus operation at point 'A' corresponds to a rectifier with unity power factor because V_s and I_L are in phase. Similarly at point 'B' operation corresponds to an inverter again with unity power factor. The straight line 'AB' is the desired steady state operation

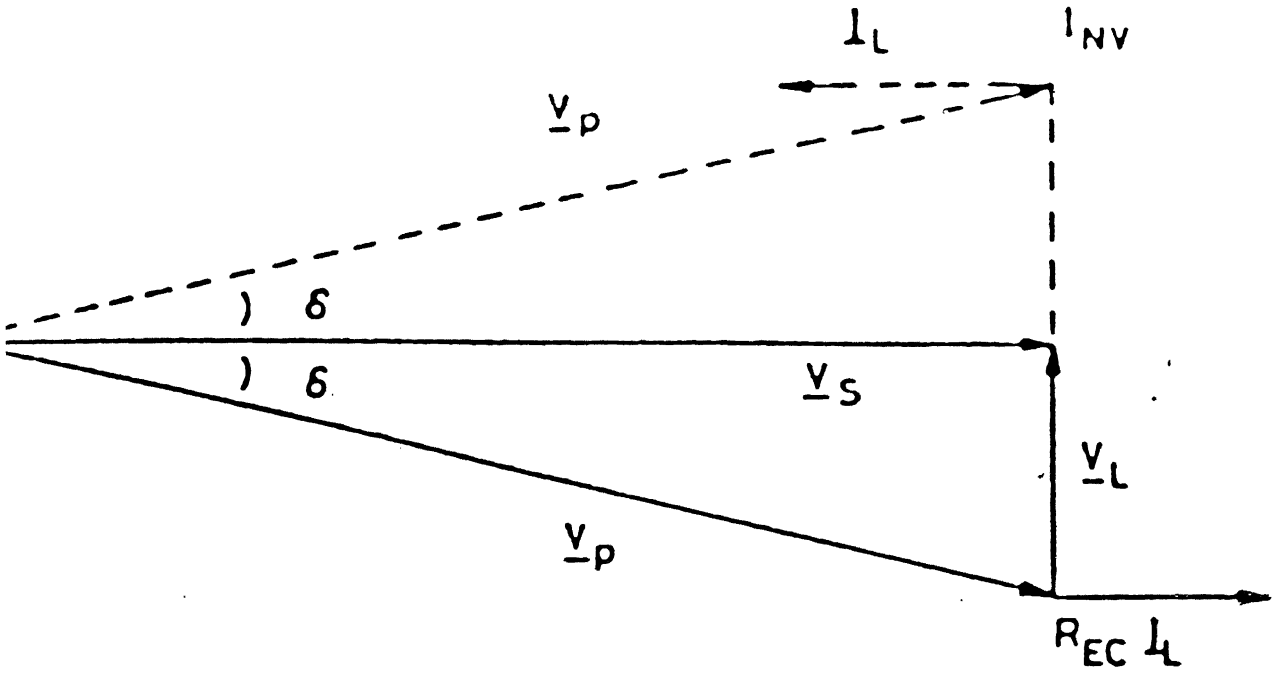


(a) Single phase equivalent



(b) Three phase equivalent

Fig. 3.1 Equivalent circuit of bidirectional converter system.



– inverting —— rectifying

FIGURE 3.2: Phasor diagram showing steady state operation of Bidirectional Power Converter.

locus for the converter for different levels of power flow at unity power factor. It can be seen from the phasor diagram that,

$$V_s = V_p \cos\delta \tag{3.1}$$

The power that flows between AC side and DC side can be given as

$$P_{ac} = \frac{3V_s V_p}{X_L} \sin\delta \tag{3.2}$$

$$X_L = \omega L_s \tag{3.3}$$

The power consumed in DC side is given as

$$P_{dc} = E_{dc} \cdot I_d \tag{3.4}$$

For maintaining the DC voltage constant the real power transferred from the supply must equal that transferred to the capacitor and load. Hence,

$$P_{dc} = P_{ac}$$

$$\text{Or} \quad \frac{3V_s V_p}{X_L} \sin\delta = E_{dc} I_d$$

$$\text{Or} \quad V_p \sin\delta = \left\{ \frac{E_{dc} X_L}{3V_s} \right\} I_d \tag{3.5}$$

Equations (3.1) and (3.5) can be simplified to give,

$$V_p = \sqrt{\left\{ \frac{E_{dc} X_L}{3V_s} \right\}^2 I_d^2 + V_s^2} \tag{3.6}$$

$$\tan\delta = \left\{ \frac{E_{dc} X_L}{3V_s^2} \right\} I_d \tag{3.7}$$

Equations (3.6) and (3.7) show that for maintaining unity power factor at the source terminals, V_p and δ are functions of DC link current I_d and DC link voltage E_{dc} (provided other factors like V_s,

X_L are constant). If the power balance is ensured at every instant of time then E_{dc} also becomes constant. Under this condition, V_p and δ become function of single parameter I_d.

From the above discussion it is concluded that the problem of maintaining unity power factor at source end reduces to finding means of varying the magnitude and phase of the PWM voltage V_p with respect to supply voltage in accordance with Eqn.(3.6) and (3.7) for varying load conditions.

3.3 CONTROL SCHEMES FOR UNITY POWER FACTOR OPERATION OF BIDIRECTIONAL POWER CONVERTER

As described in Section 3.2, the supply power factor can be maintained unity, under all loading conditions, by varying the amplitude and phase of PWM voltage V_p with respect to V_s according to Eqns.(3.6) and (3.7). There are various ways of satisfying these conditions. But the control has to be a real time control, because loading conditions of DC side can vary at any time and has to be taken in to consideration. The block diagram of the control scheme used is given in Figure 3.3.

The bidirectional power converter, when used as a rectifier, is connected between a fixed frequency, AC source (3 phase) and a constant voltage DC side. For fixed frequency source voltage, the frequency of PWM voltage (fundamental frequency of V_p must be equal to the frequency of the source V_s) has also to be constant. For fixed sampling and inverter frequency, the switching pattern is fixed for a particular modulation index (sinusoidal PWM) and can be stored in a ROM for different modulation indices, instead of calculating it again and again. ROM_3 contains status of various switches against time for

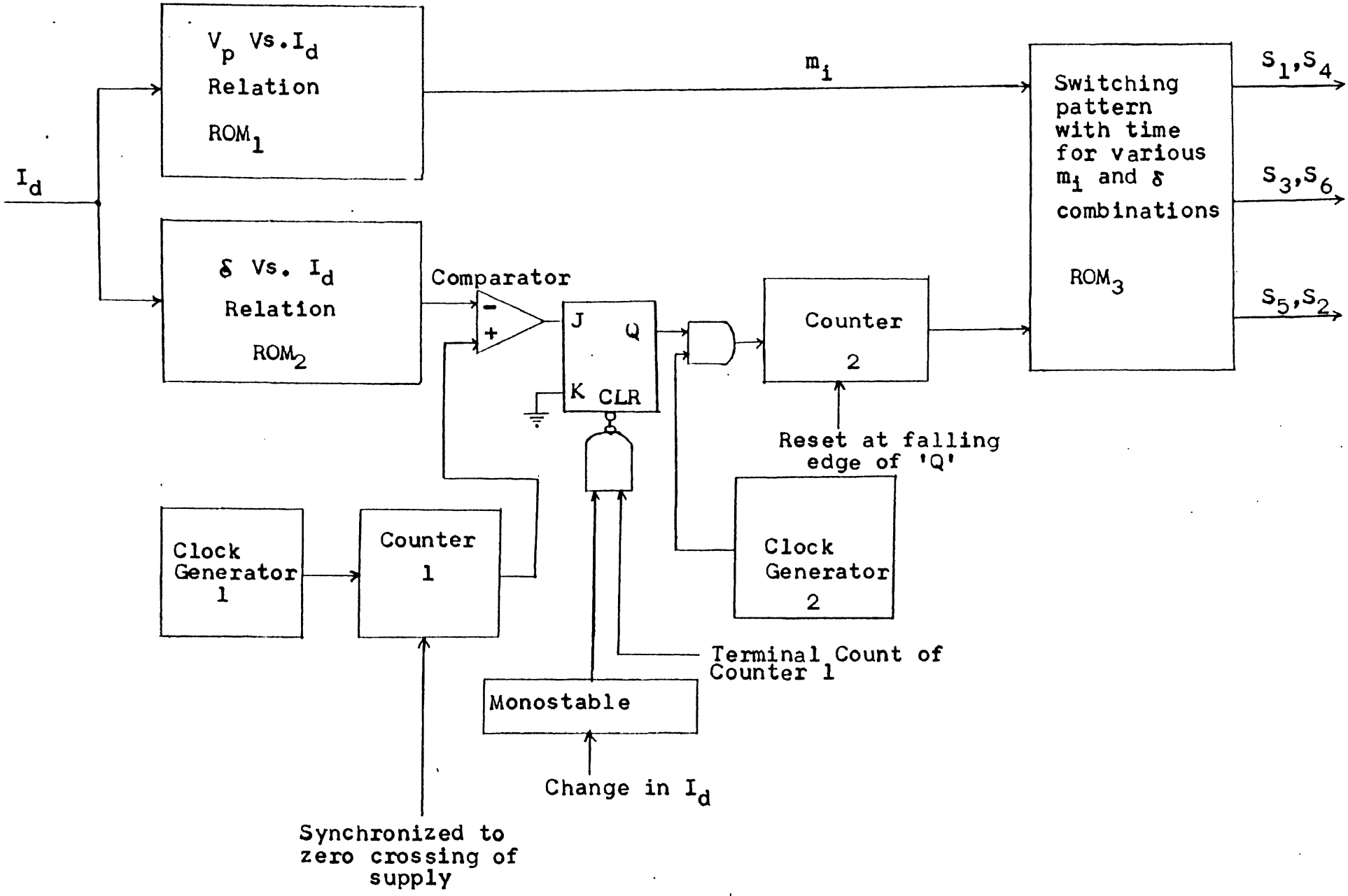


FIGURE 3.3 : Control Scheme for Bidirectional Power Converter.

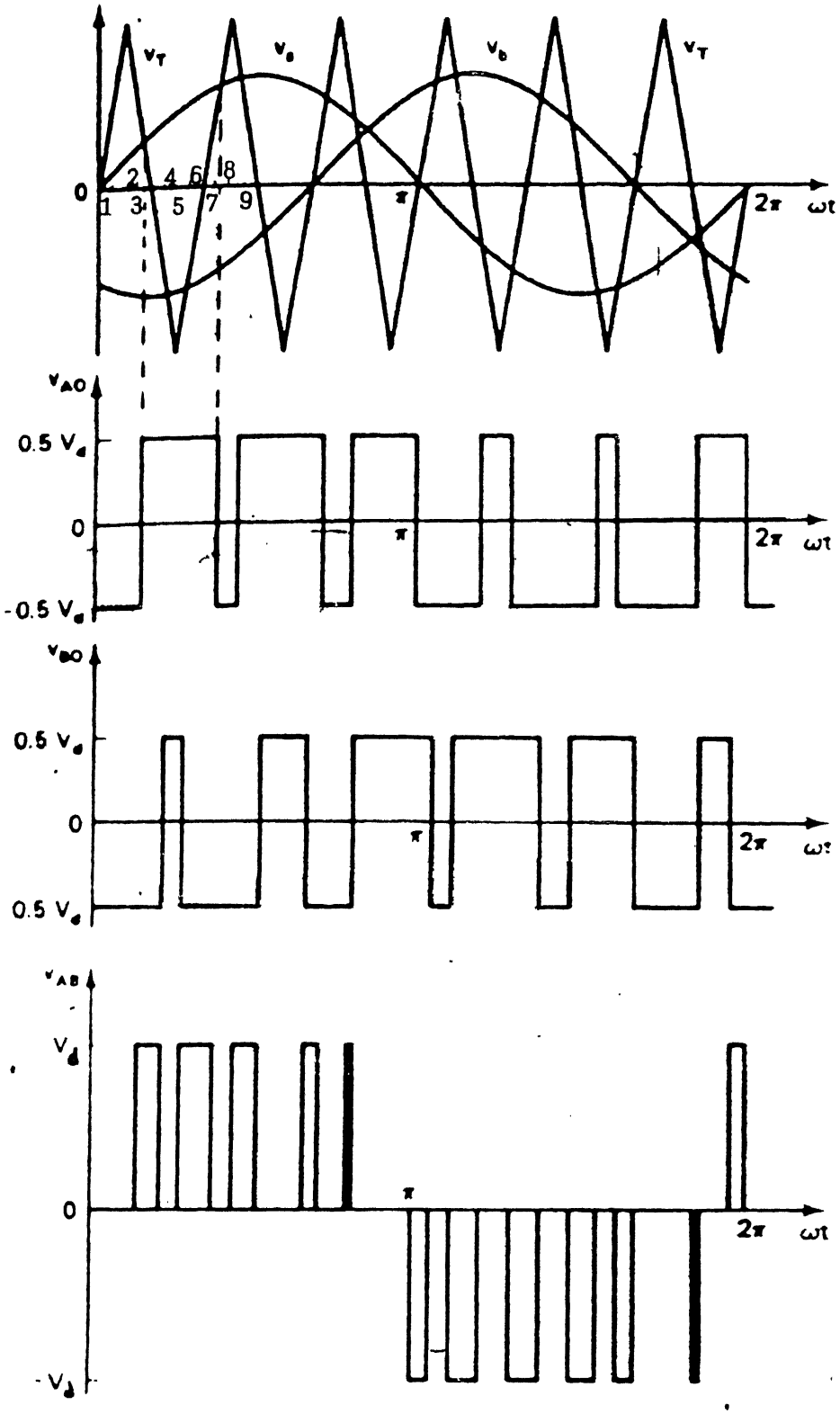


FIGURE 3.4 : Sinusoidal pulse width modulation.

different modulation indices. The total storing space of ROM is divided into a number of subsections, one for each modulation index. Considering a particular sub sector of memory space where the switching pattern for a particular modulation index is stored against time, the storage procedure is explained here.

Figure 3.4 shows the status of switches S_1 and S_4 at various time instants for sinusoidal PWM. Complete cycle can be broken into a number of parts (represented by numbers in figure). If 'ON' status of a switch is represented, by 1 and 'OFF' by '0' then for various time instants the status is given below :

Time instant	T_1	T_4
1	0	1
2	0	1
3	0	1
4	1	0
5	1	0
6	1	0
7	1	0
8	0	1
9	0	1
⋮	⋮	⋮

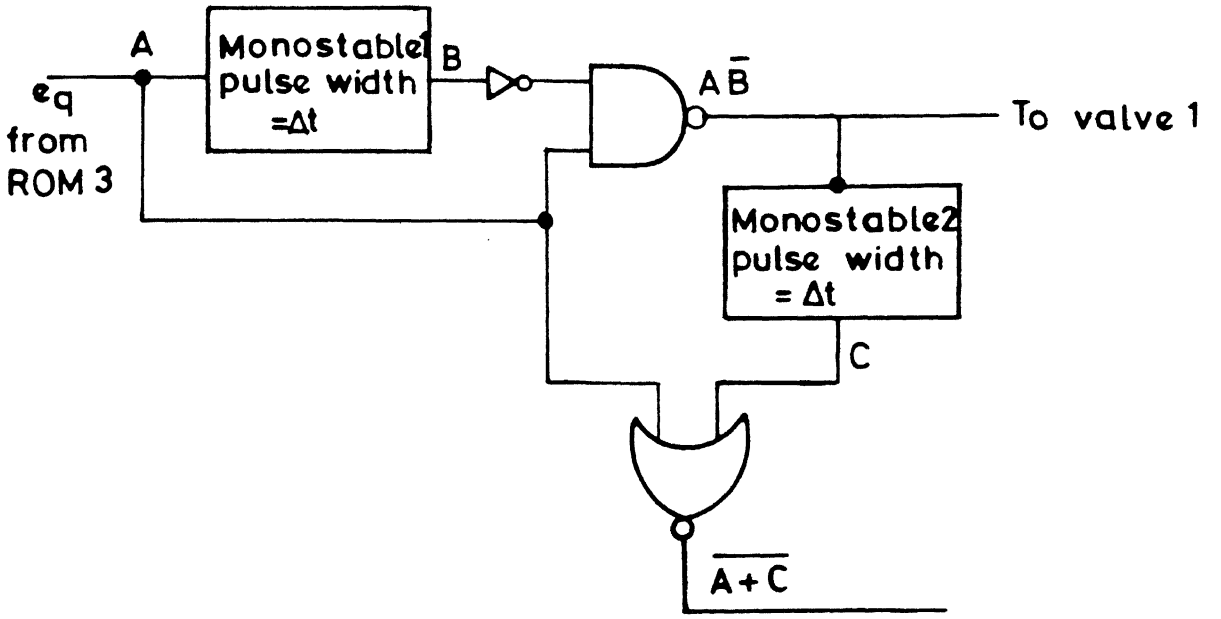
This information is stored in same way in sub-sector of ROM_3. Now higher address bits of ROM_3 represent modulation index while lower address bits represent time. The remaining part of control circuit of Figure 3.3 is to generate proper modulation index and time for ROM_3.

Modulation index (m_i) versus I_d, and δ versus I_d relations are stored in ROM_1 and ROM_2 respectively. The DC link current is sensed from the power circuit and after conditioning it is used to read values of δ and m_i from these ROMs. Modulation index is directly fed to higher address bits of ROM_3, while δ information is used to provide required phase between V_p and V_s.

Clock generator 1 and counter 1 work as a time measuring devices. Counter 1 is synchronised to zero-crossing of the supply voltage. Then it counts in such a way that after every degree in a voltage supply cycle, count increases by 1. The comparator compares the δ requirement from ROM_2 and the actual real time passed.

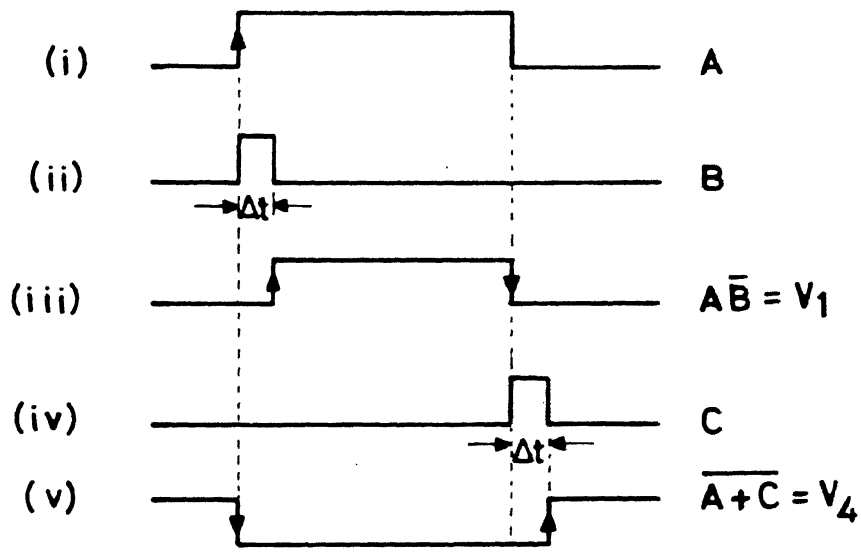
Clock generator 2 and counter 2 are used to address the lower address bits of ROM_3. Frequency of clock generator 2 is selected in such a way that count of counter 2 increases by 1 after every sampling instant. If we neglect a phase shift (δ) arrangement for a moment then clock generator 2 and counter 2 give a measure of time passed and ROM_1 give modulation index. So at the output of ROM_3 we get required switching information continuously with time.

Required phase shift between V_s and V_p is obtained by stopping passage of clock pulses from generator 2 to counter 2 for a short duration. This is achieved by the use of AND gate. If DC link current I_d changes, then the output of ROM_2 (δ) changes. The change in I_d also clears J.K. flip-flop at zero crossing of V_s (Same as terminal count of counter 1). This prevents clock pulses 2 to enter counter 2 and temporarily the time counting bits of ROM_3 stop and output of ROM_3 is zero. When real time exceed δ from zero



Δt = time gap required between
turn off of one valve &
turn on of other valve in the
same pole $\geq 2.5\, t_q$

Fig. 3.5 Minimum Dwell time limit.



(i) Pulse from ROM3 corresponding to valves 1 & 4

(ii) Monostable 1 output

(iii) Firing pulse of valve 1

(iv) Monostable 2 output

(v) Firing pulse of valve 4

Fig. 3.6 Firing pulse for valve 1 & 4

crossing of V_s the output of comparator becomes 1, setting J.K. flip-flop. AND gate gets enabled and pulses start arriving at counter 2 and it starts counting from zero and we start getting V_p at the output of ROM_3.

The PWM waveform thus starts after δ degrees have passed from zero-crossing of supply voltage, thus giving a δ degree phase shift. Counter 2 is reset at falling edge of 'Q' of J-K flip-flop to start the V_p cycle from zero after AND gate is enabled.

The output of ROM_3 can be used either directly (in MOSFET) or after proper amplification (Power Transistor) for driving the self commutated devices. Three ROMs are required in ROM_3 for the switches 1,3,5. Information for the switches 2,4,6 can be obtained by simple inversion of information of the other switch in same leg. But simple inversion means that we are trying to turn the switch 'ON' at the same instant when the other switch in the same leg is given turn off pulse. The turn off of any device takes time so for a short duration both the switches of a leg may conduct, leading to a shoot through fault. To avoid this, there must be a definite time gap between the instant when one switch is turned off and other switch in same leg is given a turn ON pulse. This can be achieved by a simple arrangement of Figure 3.5.

ROM_3 gives switching information for three legs of the bidirectional power converter. To use this information for turn 'ON' and turn 'OFF' of switches, the arrangement of Figure 3.5 is connected in each of three output lines of ROM_3. How the required firing pulses are obtained is shown in Figure 3.6 and explained below.

Monostable 1 is a rising edge triggered device which gives a pulse of specific duration Δt at the rising edge of the pulse as shown in (ii) of Figure 3.6. It is inverted and AND gated to get firing pulses for valve 1. Monostable 2 is a trailing edge triggered device which gives a pulse of duration 'Δt' at the falling edge of pulse V_1 as shown in (Iv) of Figure 3.6. It is NOR gated with main pulses of ROM_3 to give firing pulse of switch 4. Now comparing V_1 and V_4 we note that we have achieved a condition where there is a time gap Δt between turn 'ON' and turn 'OFF' instants of the valves 1 and 4. A similar arrangement is used in other two output lines of ROM_3 for other two legs of the bridge. After isolation these 6 informations can be used to drive the 6 switches of the converter.

3.4 SELECTION OF INDUCTOR

For the device to operate successfully, it is important that suitable inductors are chosen. To reduce the magnitude of the current harmonics and to facilitate smooth control a reasonably large inductance is required. Moreover, the inductors should be large enough so that the voltage drop across them is considerably more than on state voltage of the self commutating switches, otherwise the current will be distorted. On the other hand, high inductor means more cost and the dynamic range of controller has to be widened to obtain the satisfactory response. Absolute maximum value of L_s can be obtained from Eqn. (3.6) as,

$$L_{smax} = \frac{3\, V_{pmax}\, V_s \sin(\delta_{max})}{\omega\, E_{dc}\, I_{dmax}} \qquad (3.8)$$

where, $$\delta_{max} = \cos^{-1}\left\{ \frac{V_s}{V_{pmax}} \right\} \qquad (3.9)$$

CHAPTER 4

BIDIRECTIONAL CONVERTER CONTROL REALIZATION AND EXPERIMENTAL RESULTS

4.1 CONTROL REQUIREMENTS FOR THE EXPERIMENTAL CONDITION

The parameters given for the design of control circuit are a d.c. current varying from 0 to 10 Amperes, source of 60V and constant DC side voltage of 200V.

If the modulation index is not allowed to exceed unity, then we get sinusoidal pulse width operation. The PWM voltage and DC side voltage are related by

$$V_p = \frac{m\, E_{dc}}{2\sqrt{2}} \tag{4.1}$$

The maximum modulation index permitted is m=1 for sinusoidal PWM operation. So the maximum V_p attainable is,

$$V_{pmax} = \frac{E_{dc}}{2\sqrt{2}} = 70.71\ V \tag{4.2}$$

From Eqns. (3.8) and (3.9) , we get

$$\delta_{max} = \cos^{-1}\left(\frac{V_s}{Vpmax}\right) = 31.95^{\circ} \tag{4.3}$$

$$L_{smax} = \frac{3\, V_{pmax}\, V_s\, \mathrm{Sin}(\delta_{max})}{\omega\, E_{dc} \cdot I_{dmax}}$$

$$= \frac{3 \times 70.71 \times 60 \times \mathrm{Sin}\ 31.95}{100 \times 200 \times 10}$$

$$= 10.72\ \mathrm{mH}.$$

The value of L_s selected is 10 mH. The basic governing equations for the control circuit under above stated parameters becomes [from Eqns.(3.6) and (3.7)],

$$V_p = \frac{m\,E_{dc}}{2\sqrt{2}} = \left[\left\{ \frac{E_{dc} \cdot \omega L_s}{3\,V_s} \right\} I_d^2 + V_s^2 \right]^{1/2}$$

$$\text{Or} \quad m = \frac{1}{70.71} \sqrt{12.185\, I_d^2 + 3600} \tag{4.4}$$

$$\delta = \tan^{-1} \left[\left\{ \frac{E_{dc}\, X_L}{3\, V_s^2} \right\} \cdot I_d \right]$$

$$\text{Or,} \quad \delta = \tan^{-1} [\, 0.0581776\, I_d \,] \tag{4.5}$$

4.2 IMPLEMENTATION OF CONTROL

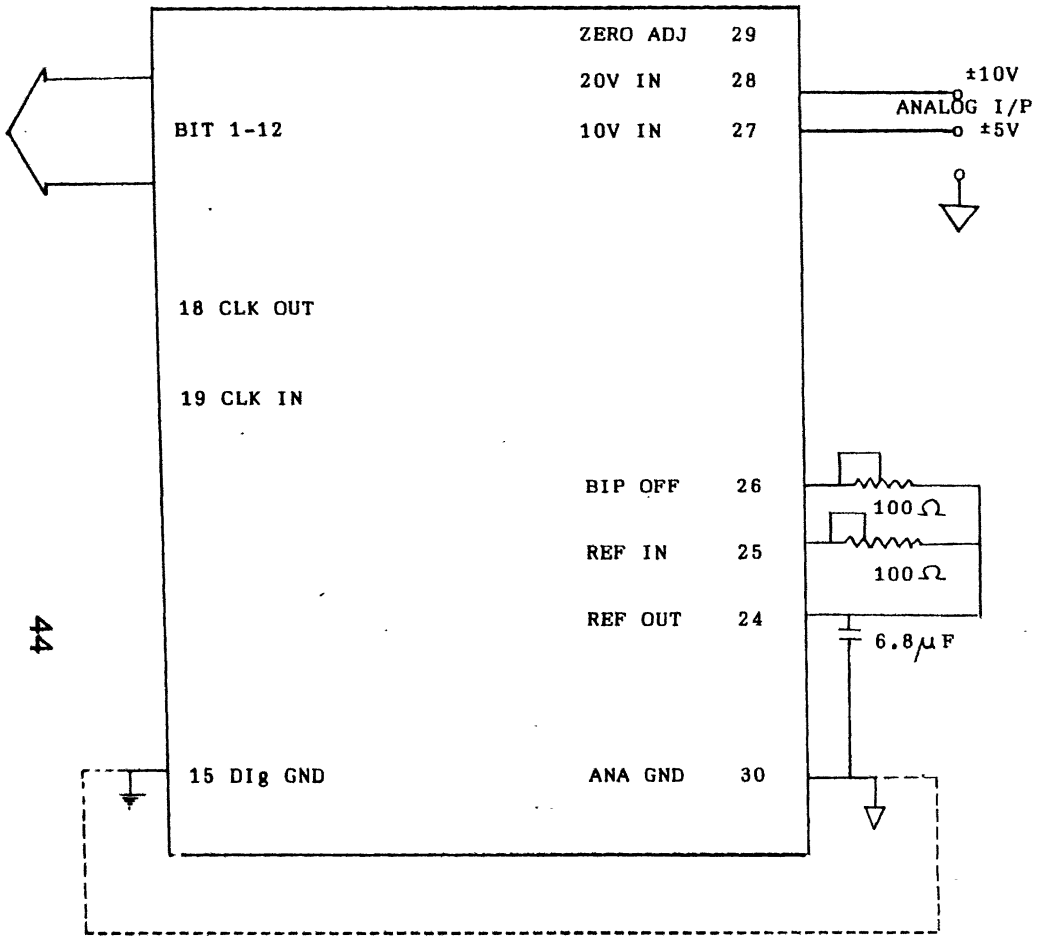
Control scheme shown in Figure 3.3 consists of a number of blocks which are implemented with hardware components. The present section discusses the implementation of different blocks separately.

4.2.1 Analog to Digital Conversion of Signal I_d

AD578 is used for A/D conversion. It is a high speed 12 bit successive approximation analog to digital converter, which includes an internal clock reference and comparator. It has a conversion time of 3 μs (max). The pin diagram and connections are shown in Figure 4.1.

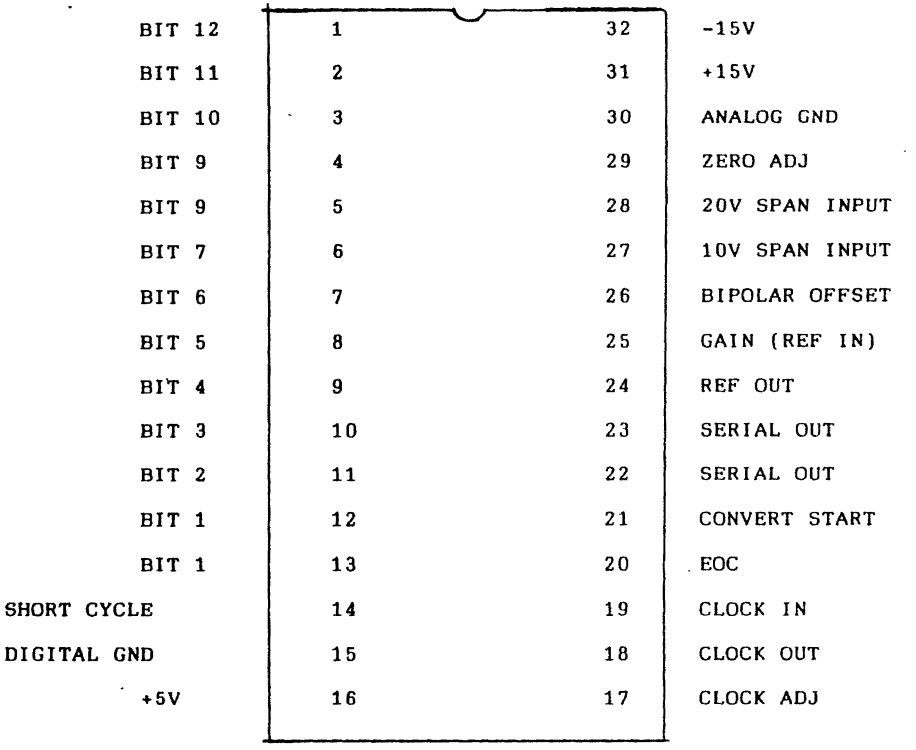
In the experiment I_d used is a 6 bit digit only, so 6 MSBs of AD578 are used. It is used as a 6 bit converter.

Since it is a successive approximation type A/D converter, the

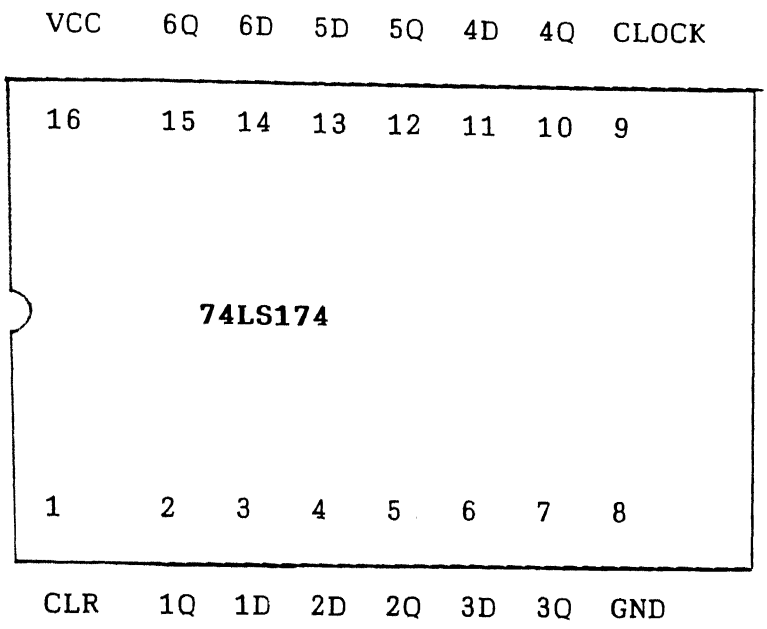


(b): BIPOLAR INPUT OPERATION

FIGURE 4.1: AD 578 connection diagram.

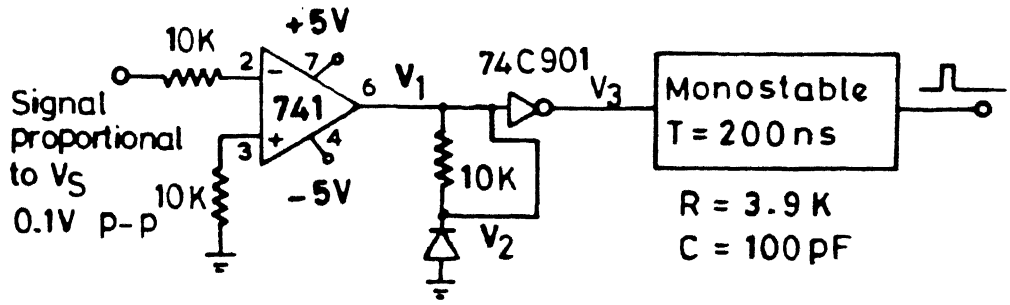


(a): Pin diagram of AD 578

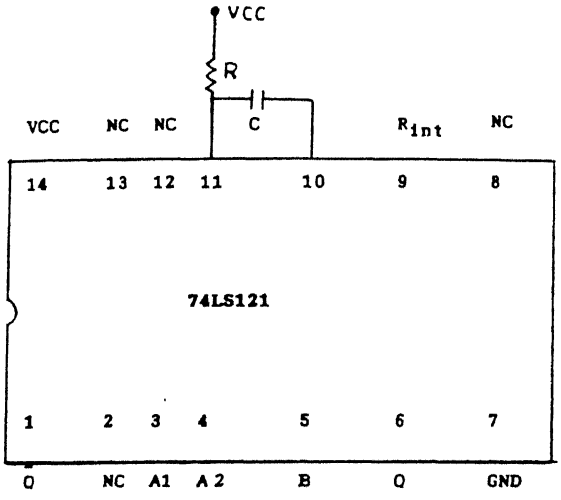


CLR	CK	D	Q_{n+1}
L	X	X	L
H	↑	L	L
H	↑	H	H
H	L	X	Q_0

FIGURE 4.2 : Pin diagram for latch 74LS174

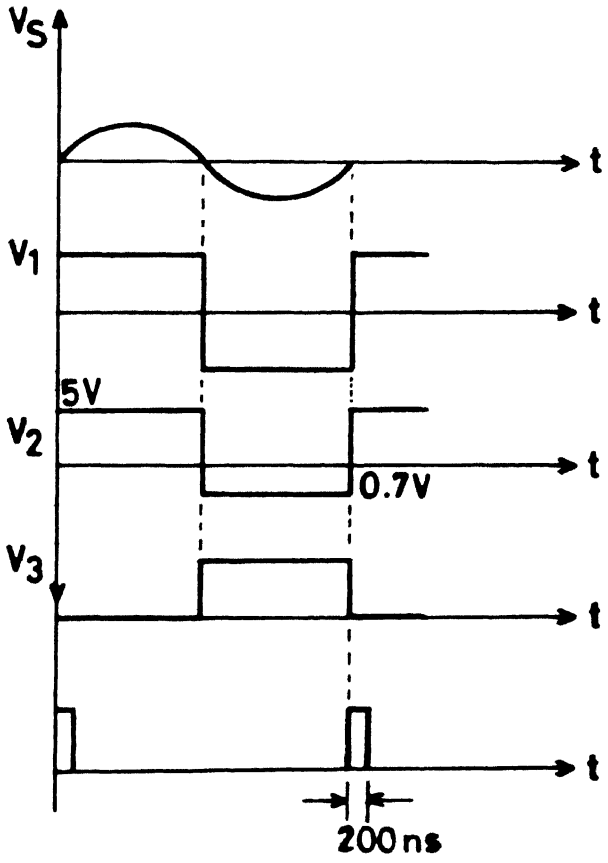


(i) SOC pulse generation at zero crossing of V_S.



A1	A2	B	Q
L	X	H	L
H	↓	H	⊓
↓	H	H	⊓
↓	↓	H	⊓
L	X	↑	⊓
X	L	↑	⊓

iii) Pin diagram of Monostable.



(ii) Various stages of SOC pulse

Fig. 4.3 Arrangement of getting SOC pulse.

output bit keeps on changing randomly between the start of conversion pulse at pin 21 and the end of conversion E_{oc} pulse from pin 20. This problem of bit fluctuation can be avoided by using a 6 bit latch at the output of A/D converter, which latches the data at falling edge of E_{oc} (i.e. when conversion is complete) till next falling edge of E_{oc}. The latch used is 74LS174, whose pin diagram and truth table is shown in Figure 4.2.

To latch data at falling edge of E_{oc}, the E_{oc} is inverted and fed to 'CK' input of the latch while 'CLR' is made high permanently. 6 bit output of A/D converter is fed to 'D' input of the latch. At falling edge of E_{oc} pulse, the clock pulse has a rising edge and data is latched in the device.

It is explained in Section 3.3 of previous chapter that any corrective action is taken only after the zero crossing of V_s. Hence, the information of I_d is to be renewed at zero crossing of V_s. For this purpose we have to give a start of conversion (SOC) pulse to A/D converter at zero crossing of supply voltage. The SOC pulse must be of 200 nS duration for AD578 to work satisfactorily. A simple circuit shown in Figure 4.3 shows the arrangement of obtaining SOC pulse.

4.2.2 Storage of PWM Pattern in ROM

The heart of control scheme is a 64 K ROM containing the switching pattern for different values of modulation indices for all three phases. Ideally three 1x64 K ROMs are required. We require only one bit to be stored in ROM (either 1 or 0). So output word length is only one. But due to non availability of 1x64 K ROM two

8x32 K ROMs are used. Since the output length is 8 and we require 1 only so switching patterns of all the three phases are stored in the same output byte. The range of modulation index for 0-10 A current range is 0.85 to 0.98 (from Eqn.4.4) but we have stored for 0.75 to 1. The frequency of triangular wave is taken as 2.5 KHz so the sampling period becomes 4×10^{-4} sec. Also the complete 64 K memory space is divided into 32 sections each of 2048 byte space. In each section we store switching pattern corresponding to one modulation index. The whole range of m_i (0.75 to 1) is divided into 32 intervals. The supply voltage cycle of 2π (20 mS for 50 Hz case) is divided into 2048 intervals for storage. So spacing between two interval becomes 20/2048 mS.

Keeping the above factors in mind, a simple computer programme is written to obtain switching pattern. It is given as under :

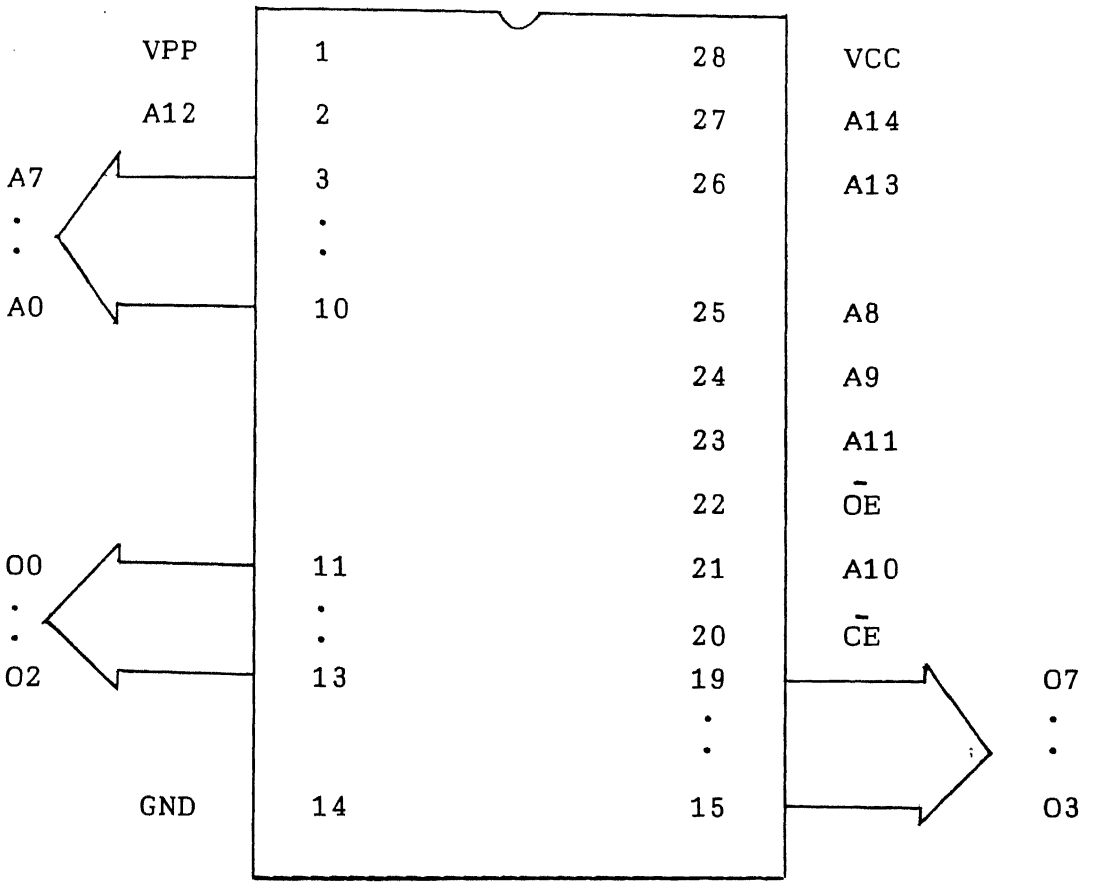
```
      DO  100        I = 1,32                 Remark
      AM  = 0.75 + (I-1)/32.00                AM ≡ modulation index
      DO  200        J = 1,2048
      T   = Jx0.02/2048.0
      T1  = T + 1./150
      T2  = T + 1./75                         1/150 sec ≡ π/3 degrees
      CALL INTER (T, AM, 00)                  1/75 sec  ≡ 2π/3 degrees
      CALL INTER (T1, AM, 01)
      CALL INTER (T2, AM, 02)
      IO =   4x02 + 2x01 + 00
      WRITE (7, 300) IO
  300 FORMAT ('DB', 3X, I1)
  200 CONTINUE
```

```
100 CONTINUE
      STOP
      END
   SUBROUTINE  INTER (T, AM, Y1)
     I = T/(4E-04)
     T = T-I * (4E-04)
     F1 = AM * SIN (100 * PI * T)          PI = π
     IF (T.LE.1E-04) F2 = (1E04)*T
     IF  (T.LE.3*E-04. AND . T.GT.1E-04 )  GO TO 10
     GO TO 20
10   T = T-1E-04
     F2 = 1-(1E04)*T
20   IF (T.LE.4E-04.AND.T.GT.3E-04) GO TO 30
     GO TO 40
30   T = T-3E-04
     F = -1 + 1E04*T
40   IF (F1.GE.F2) Y1  = 1
     IF (F1.LT.F2) Y1 = 0
     RETURN
     END
```

The ROM employed to store the data generated from the above programme is 27C256. It is a 8x32 K ROM which can be loaded on a ROM loader. The pin diagram of IC and its function table is shown in Figure 4.4.

4.2.3 Storage of Modulation Index Vs I_d Relation in ROM_1

The modulation index information should change the 5 MSB of



MODE \ PIN	$\overline{CE}$	$\overline{OE}$	VPP	VCC	O/P
READ	0	0	VCC	VCC	D_{OUT}
O/P DISABLE	0	1	VCC	VCC	HIGH Z
STAND BY	1	X	VCC	VCC	"

FIGURE 4.4: Pin diagram of 8 x 32 K ROM 27 C 256

ROM_3 address in such a way that a particular I_d generates a 5 bit address which correctly chooses one the 32 set of switching patterns stored in main ROM_3.

It can be noticed from FORTRAN programme of Section 4.2.2 that 5 MSB of address required for $m_i = 0.75$ is 00000 (i.e. 0) and for an increment in m_i by 1/32 the address bits should increase by 1 i.e. $m_i = 0.75 + \frac{1}{32}$ the address should be 00001 and so on.

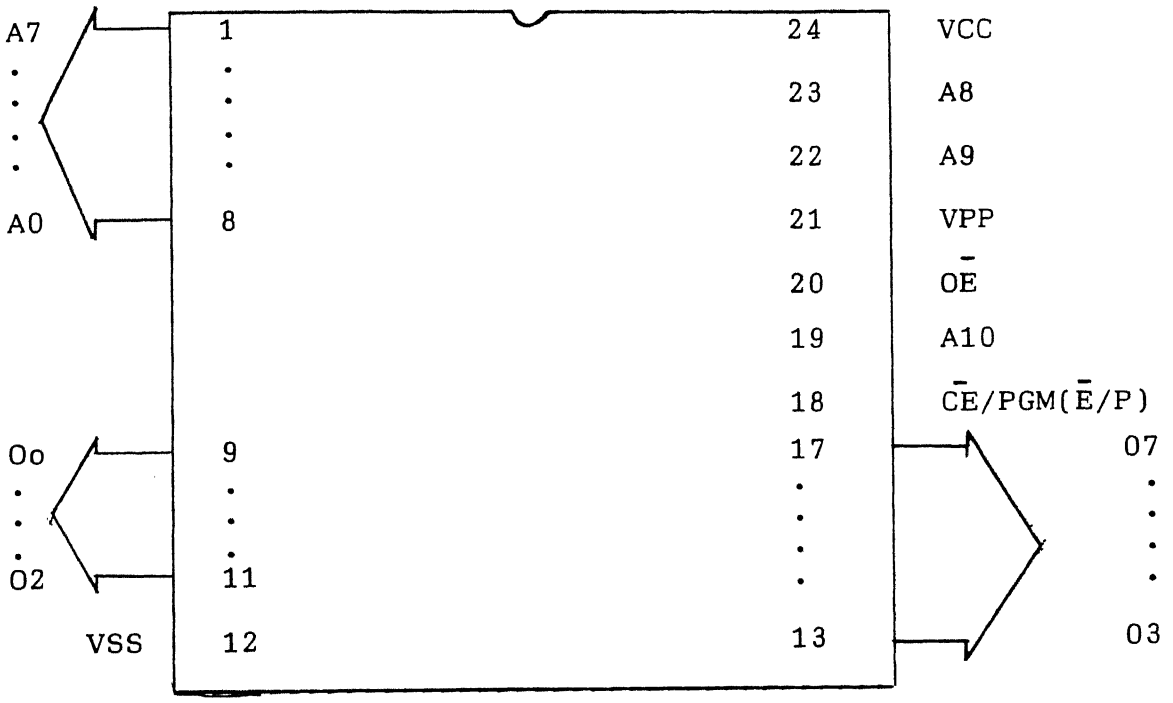
For a change in I_d from -10A to +10A the value of m_i is calculated from Eqn.(4.4) and corresponding address required is found out by

$$\text{Address} = \text{Integer of } [(m_i - 0.75) * 31] \qquad (4.6)$$

I_d is a 6 bit number and hence can have maximum of $2^6 = 64$ states starting from 000000 for -10A to 111111 for +10A. For every state of I_d the corresponding MSB address of ROM_3 (containing switching pattern) is found out using Eqns.(4.4) and (4.6). This information is stored in a 5x64 bit ROM [ROM_1 of Figure 3.3]. However, due to non-availability of such a ROM 8x2 K ROM (IC 2716) is used. Its pin diagram is shown in Figure 4.5.

4.2.4 Time Address Generation Of ROM_3

ROM_3 is a 64 K ROM having 16 bit address line. The first 5 MSB have information regarding modulation index as described in Section 4.2.3. Remaining 11 bits are used to address ROM_3 successively after rgulr interval so that PWM information keep on arriving at output pin of ROM_3.



READ:	E/P	=	V_{IL}
	OE	=	V_{IL}
	VPP	=	5V
	VCC	=	5V

FIGURE 4.5 : Pin diagram of ROM 27C16

4.2.4(A) Clock Generation Using a PLL

It is assumed in the discussion of Section 3.3 that the supply voltage is of constant frequency of 50 Hz. But in actual practice it is never constant. It keeps fluctuating between $\pm$ 2 Hz or so. The PWM voltage V_p must have fundamental frequency exactly equal to that of V_s. It is achieved by using a PLL (phase locked loop system). Also since in a cycle 2048 memory locations of ROM_3 have to be addressed; the frequency of clock must be 2048 times the supply frequency. It is achieved by a simple scheme of Figure 4.6. The output is taken from point 'A'.

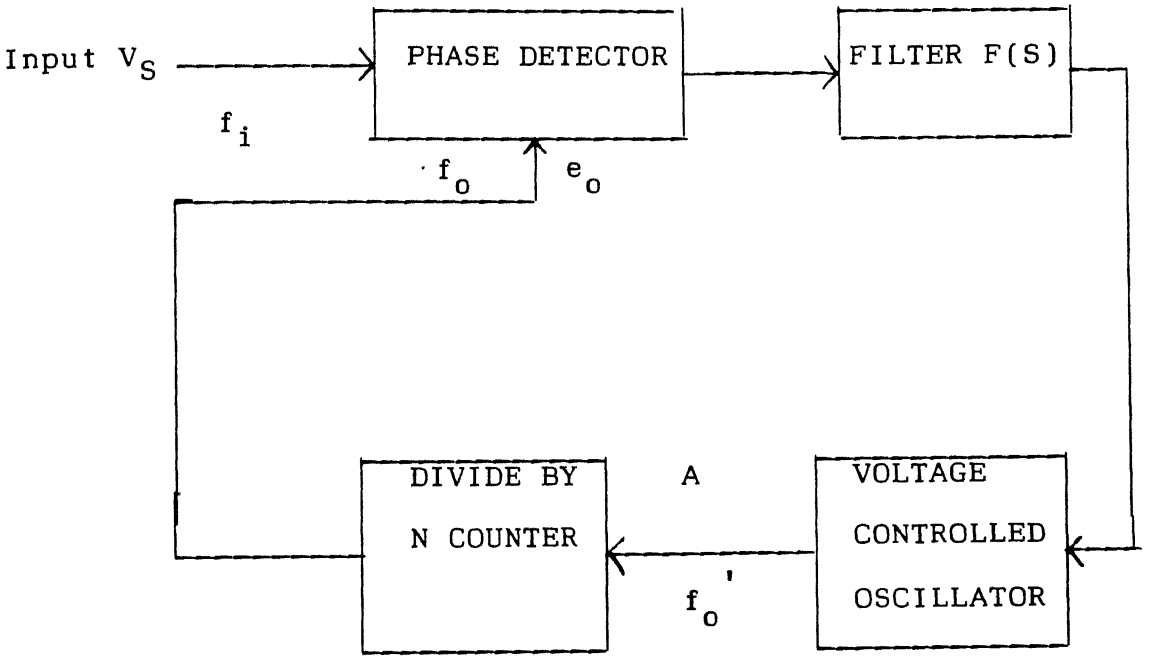
The PLL used is LM 565 CW. The pin diagram and the connections are shown in Figure 4.7.

4.2.4(B) Address Generation with Counters

We require 11 bit address which changes with time uniformly in such a way that all the 2048 memory locations of ROM_3, for a particular modulation index, are addressed in one supply cycle of 20 mS. If we use a 11 bit counter to count the pulses obtained from PLL having 2048 fi frequency then all the locations will be read in one supply cycle. Due to non-availability of 11 bit counter, three 4 bit synchronous counters are used in cascade and 12 bit counter is reset at a terminal count of 2048 (MSB of 12 bit counter is inverted and fed to CLR of all the counters) making it a 11 bit counter. The 4 bit synchronous counter used is 74LS163 which is shown in Figure 4.8.

4.2.4(C) Phase Shifting Arrangement

For unity power factor operation of bidirectional power



$$f_o = f_i$$

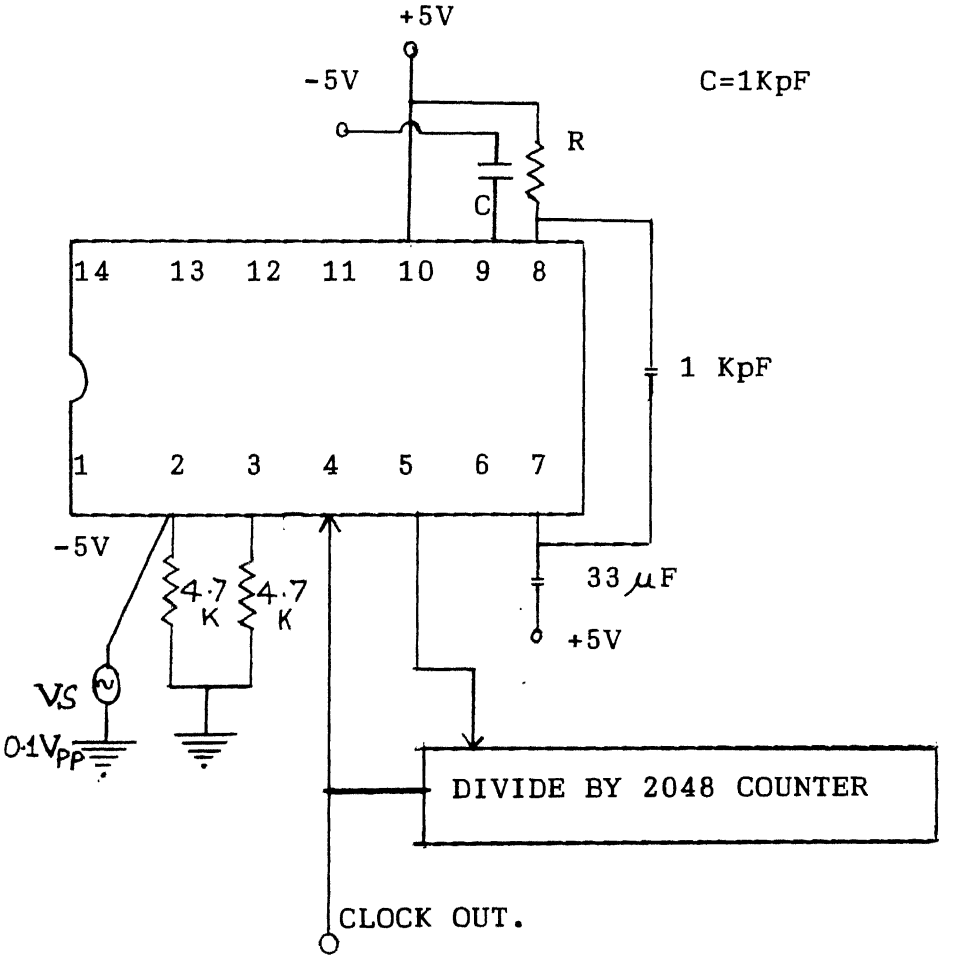
$$f_o' = Nf_o$$

$$= Nf_i$$

FIGURE 4.6 : Basic PLL for frequency multiplication.

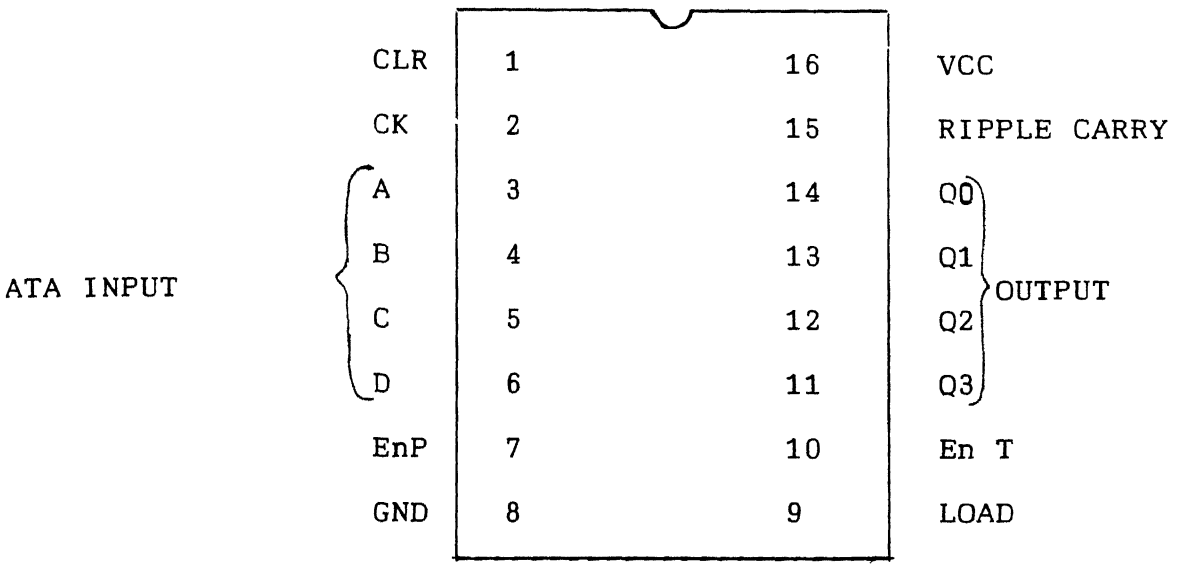
-VCC	1	14	NC
INPUT	2	13	NC
INPUT	3	12	NC
VCO OUTPUT	4	11	NC
PHASE COMPARATOR VCO INPUT	5	10	+VCC
REF. OUTPUT	6	9	TIMING CAPACITOR
VCO CONTROL VOLTAGE	7	8	TIMING RESISTOR

(a) IC 565, Phase locked loop.



(b)

FIGURE 4.7: Clock generation using PLL 565.



FOR CASCADING : Ripple carry of lower stage is connected to En T of higher stage.

FOR COUNTING:

CLR = H

LOAD = H

En P = H

En T = En T of higher stage.

FIGURE 4.8 : 4 bit synchronous counter. 74LS163.

converter Eqns.(3.6) and (3.7) must be fulfilled all the time. Modulation index control has been discussed earlier but a definite phase angle should be maintained between V_s and V_p to ensure unity power factor operation.

4.2.4(D) ROM Containing δ Vs I_d Relation

As mentioned earlier I_d is a 6 bit number, and can have only 64 states. The value of 'δ'can be calculated from Eqn.(3.7). Maximum value of δ can be 360° which requires a 9 bit byte. We therefore, require a 9x64 bit ROM. Again non-availability of such ROM led us to use a 8x2K ROM (IC 27C16 given in Figure 4.6). But now the maximum number that an output byte can represent is only $2^8 - 1 = 255$. Therefore, angle obtained from Eqn.(3.7) is converted using expression,

$$\text{New angle} = \frac{256}{360} * [\text{Angle obtained from Eqn.(3.7)}] \qquad (4.7)$$

This angle is stored for all the 64 values of I_d (-10A to +10A) in a ROM (ROM_2 of Figure 3.3)

4.2.4(E) Angle Counter

A clock of frequency 256 fi is obtained by dividing main clock of PLL (having frequency 2048 fi) by 8 using a 4 bit counter reset at a terminal count of 8 (MSB connected to clear input after inversion). This clock of frequency 256 fi is counted by a 8 bit counter (two 4 bits counters connected in cascades). The counter is cleared at zero-crossing of the supply voltage. For this SOC (start of conversion) pulse of A/P converter is fed to CLR input of counter after inversion.

This clock and counter arrangement work as an angle counter which counts the actual degrees passed from zero crossing of supply voltage. It works as a reference for providing 'δ' delay in V_p with respect to V_s.

4.2.4(F) Change of I_d Sensor

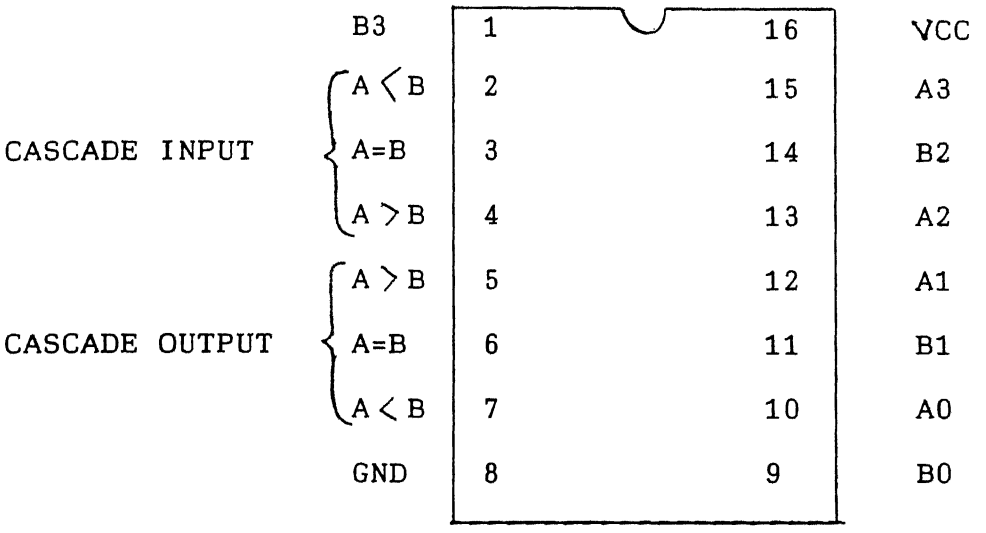
As mentioned in Section 4.2.1 the I_d value remains fixed from falling edge of one EOC pulse to other. If we store the I_d value of previous cycle before renewing it at the falling edge of EOC, then we have information for two cycles, which can be compared to get any change in I_d. There is definite time interval between rising edge of SOC pulse and falling edge of EOC. So we latch the I_d data at rising edge of SOC pulse into a 6 bit latch (74LS174).

The renewed value of I_d and the latched values are compared in a 6 bit digital comparator. Two 4 bit comparators (74LS85) are cascaded to give a 8 bit comparator. A 4 bit comparator is shown in Figure 4.9.

4.2.4(G) Comparator, Latch and Enable Gate

The output of ROM_2 'δ' (8 bit) and output of angle counter (8 bit) are compared in a 8 bit digital comparator, consisting of two 4 bit comparators in cascade. This assumes a high value whenever the angle counter's output exceeds 'δ'. This information is latched in a J.K. flip-flop as shown in Figure 4.10. The flip-flop is cleared whenever there is a change in I_d at zero crossing of supply voltage.

How the comparator, J.K. flip-flop and enable gate assembly



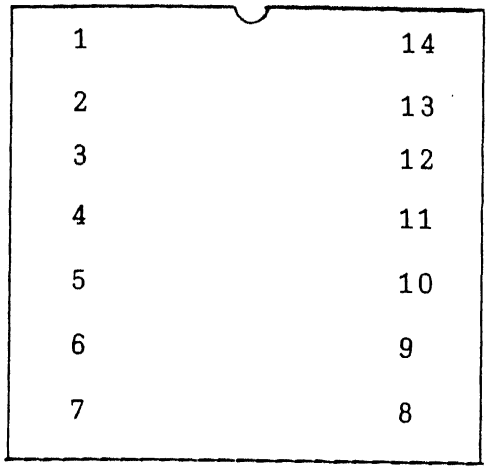
FOR CASCADING : A > B, A=B & A < B outputs of lower stage is connected to corresponding cascade input of the higher stage.

The cascade inputs of least significant position unit are connected as :

$I_{A<B} = I_{A>B} = L$

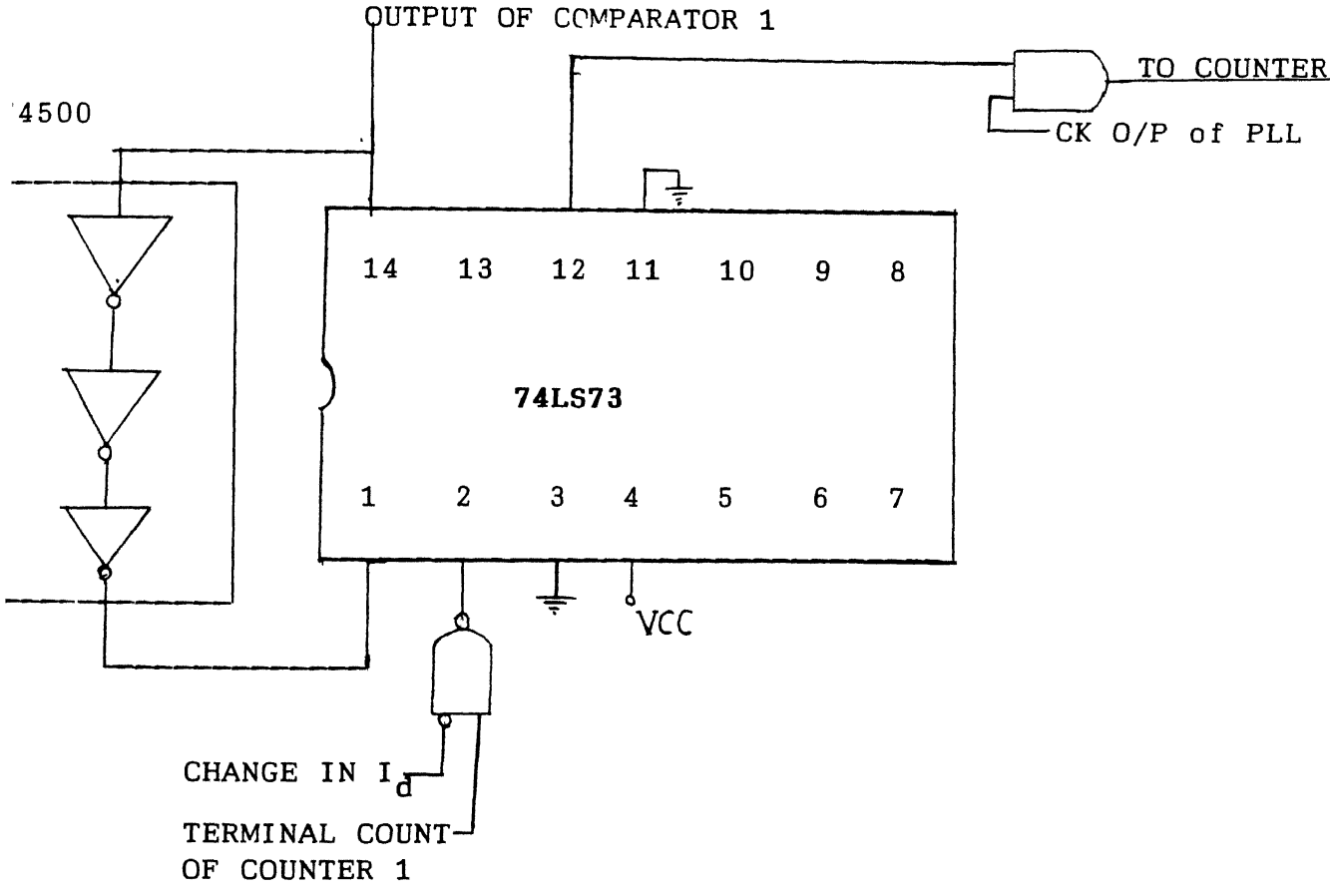
$I_{A=B} = H$

FIGURE 4.9 : 4 bit digital comparator 74LS85.



CLR	CK	Q
L	X	L
H	H	R^0
H	↓	WORKS AS JK FLIP-FLOP

(a) Pin diagram of IC 74LS73



[GURE 4.10 : Use of JK flip-flop and enable gate in phase shifting.

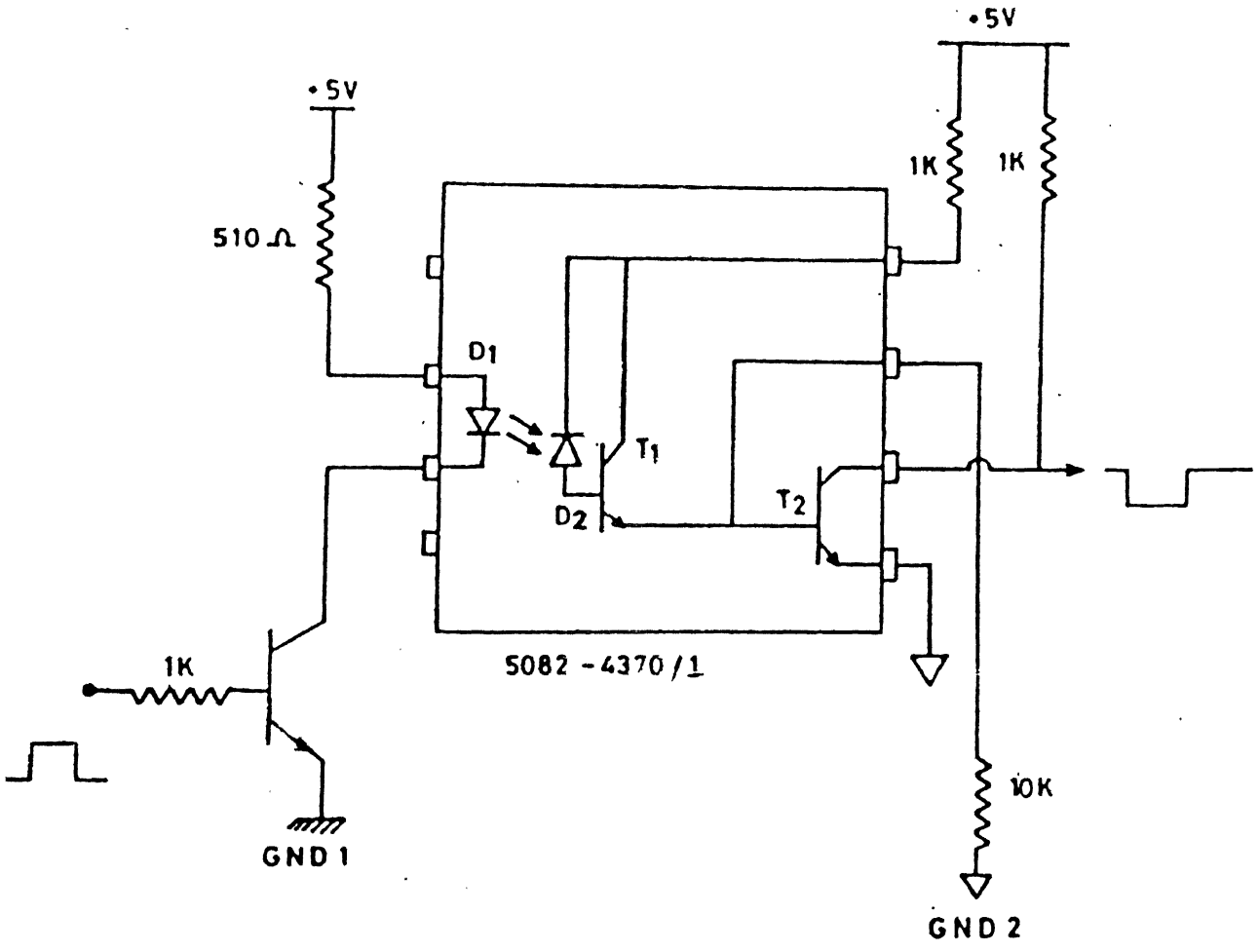


FIGURE 4.11 : Opto-Isolator.

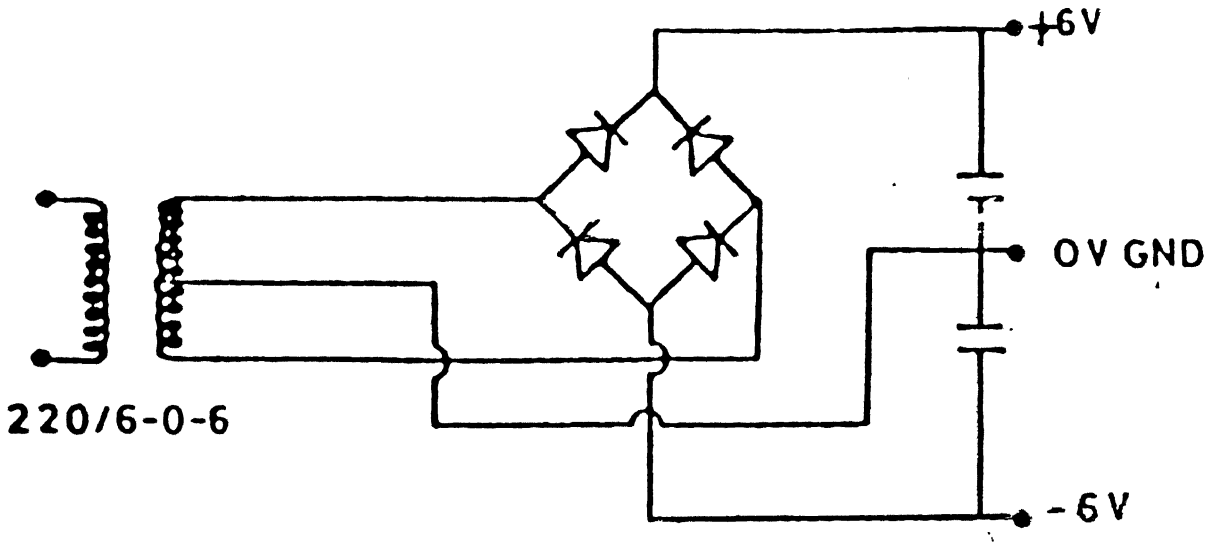


FIGURE 4.12 : Power Supply.

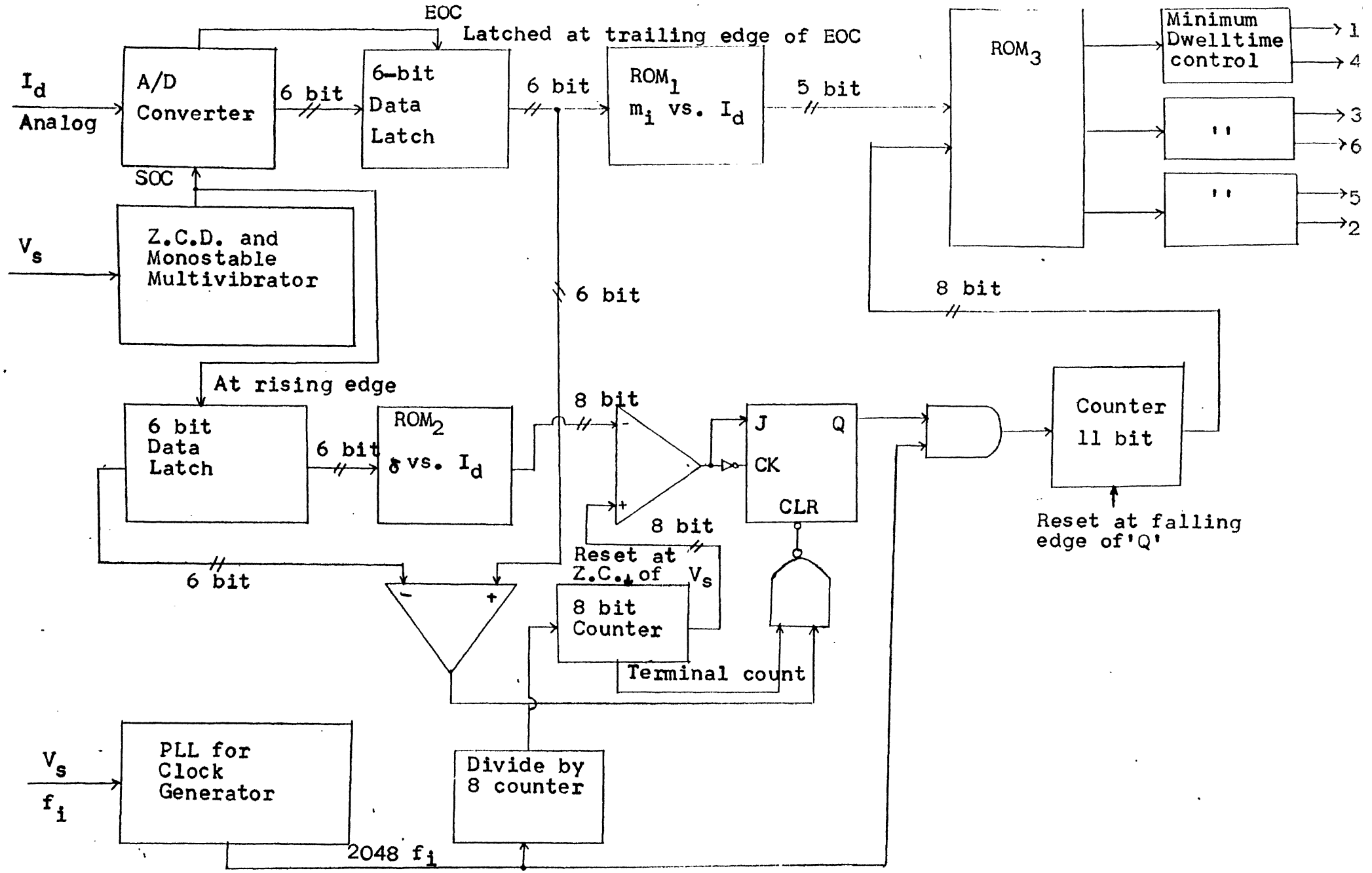


FIGURE 4.13 : Control scheme for bidirectional power converter.

works in providing phase shift is already explained in Section 3.3 of the previous chapter.

4.2.4(H) Minimum Dwell Time Unit

It is shown in Figure 3.5 of Chapter 3 and its operation is also explained in Section 3.3 of the same chapter.

4.2.4(I) Isolation Circuit

All the 6 firing pulses obtained from control circuit are with respect to single ground of the control circuit. So they cannot be directly connected to gates of various switches. An isolation stage is essential between control and power circuits.

Isolation in this case is obtained by an opto isolator (Figure 4.10 shows such a current isolator chip 5082-4370/1).

Whenever there is a high pulse at the input D_1 conducts and emits light. D_2 (a photo diode) starts conduction as light strikes it and provides, base current to T_1, which drives T_2. As T_2 goes into conduction the output goes low. Whenever input pulse is low, D_1 does not conduct, thus transistors go into off state and output becomes high. For the output of isolator to be isolated from input, the output supply is separate.

Figure 4.12 shows the separate power supply. For this purpose a transformer (220/6.3-0-6.31 A) with a bridge rectifier and a capacitor filter is used.

4.3 EXPERIMENTAL RESULTS

The control circuit is tested for various values of DC link

current I_d. The waveforms at various points of control circuit are photographed with a high speed film.

As explained in Section 4.2.1 the analog to digital conversion of I_d requires a start of conversion pulse of width 200 nS at the positive going edge of source voltage, V_s. The circuit required for this and expected waveforms are shown in Figure 4.3. The waveforms obtained experimentally are given in Figures E1 and E2. Figure E1 shows the reduced source voltage V_s (100 mV peak to peak) and output of zero crossing detector. This is used to trigger a monostable having time period of 200 nS. The SOC (start of conversion pulse) and the source voltage are shown in Figure E2.

Section 4.2.4(A) gives the method of clock pulse generation using PLL (phase lock loop). The source voltage V_s (reduced 100 mV p-p) and the output of PLL are shown in Figure E3. From the figure it is observed that the frequencies of both the waveforms are identical. The frequency of clock has to be 2048 times that of supply voltage. The waveform at point (A) of Figure 4.6 is used as a clock for further circuit. It is shown in Figure E4. Due to the characteristics of VCO (voltage controlled oscillator) the waveform is distorted at rising and falling edge. Also the rising edge is having some negative spike (clearly visible in Figure E4). These pulses cannot be fed to further circuit as spikes will lead to malfunctioning. A buffer is employed to give the pulses a clear shape. The buffered dock is also shown in the same figure (E4).

Final control pulses of the three legs of the converter are shown in Figure E5 for a DC link current of 3.6 A in rectification

mode. It shows that these pulses are displaced by 120° from each other.

Each of these pulse trains is passed through the circuit of Figure 3.5 to impose minimum dwell time limit. The pulses of the two switches of same legs must be displaced by 1 μSec to allow time for successful turn off. The pulses for switches 1 and 4 of leg 'a' of Figure 2.2 are given in Figure E6 for a DC link current of 4 A. Its enlarged version (magnification of 5 in time axis) is shown in Figure E7. It can be seen from the figure that there is a shift between turn off pulse of switch 1 and turn on pulse of switch 4.

The source voltage V_s and the synthesized PWM voltage of phase 'a' for $I_d = 0$ are shown in Figure E8. It is seen from the figure that the peak of V_s and the most closely spaced pulses of V_p occur together. Similarly the negative peak of V_s occurs at the same instant when the thinnest pulse of V_p occur i.e. a phase difference of 0° is there. This confirms that the requirements of the control circuit are met.

Figure E9 and E10 show the photograph of the source voltage of phase 'a' and the PWM voltage of phase 'b' for DC current of 10 A (E9 for rectification and E10 for inversion). It can be seen from the figures that the source voltage and PWM voltages are not in phase. It is not easy to determine phase shift from the figure as one waveform is sinusoidal while the other is pulse width modulated. However, if we assume the maximum closely placed pulse point as peak of fundamental the phase shift for rectification is roughly 31° while that for inversion is approximately 37°. From Eqn.(4.5) the angle

must be 30.2°. The variation in values is mainly due to highly approximate method of phase angle measurement and inaccurate measuring of DC side current.

However, these figures broadly confirm the operation of the control circuit as per requirement.

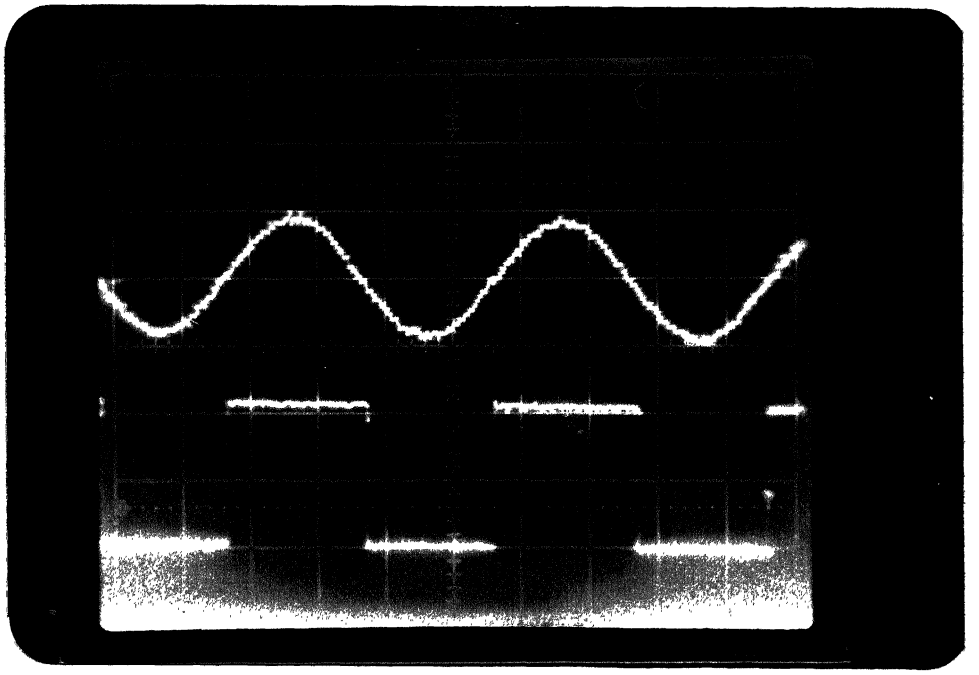


FIGURE E1 : Zero crossing dectection of source voltage V_s

(i) Reduced Supply Voltage

50 mV/div, 5 mS/div

(ii) Output of zero crossing detector

2 V/div, 5 mS/div.

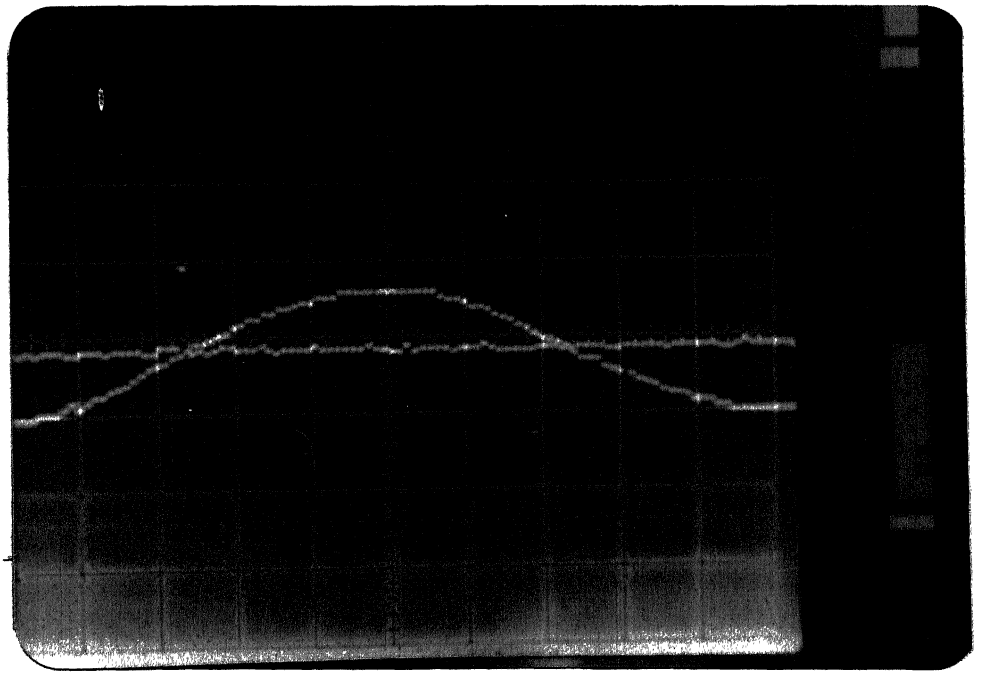


FIGURE E2 : Analog to Digital conversion of I_d

(i) Reduced Supply Voltage

50 mV/div, 5 mS/div

(ii) Start of conversion (SOC) pulse for ADC

2 V/div, 2 mS/div.

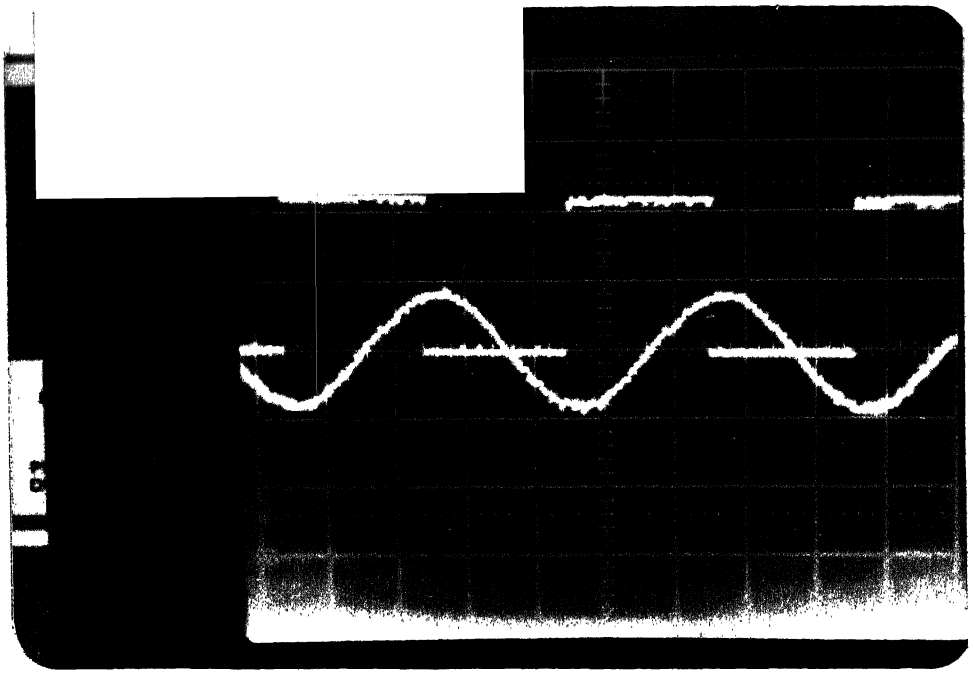


FIGURE E3 : Frequency locking of V_s and V_p using PLL

(i) Reduced supply voltage

50 mV/div, 5 mS/div

(ii) Output of PLL

2 V/div, 5 mS/div.

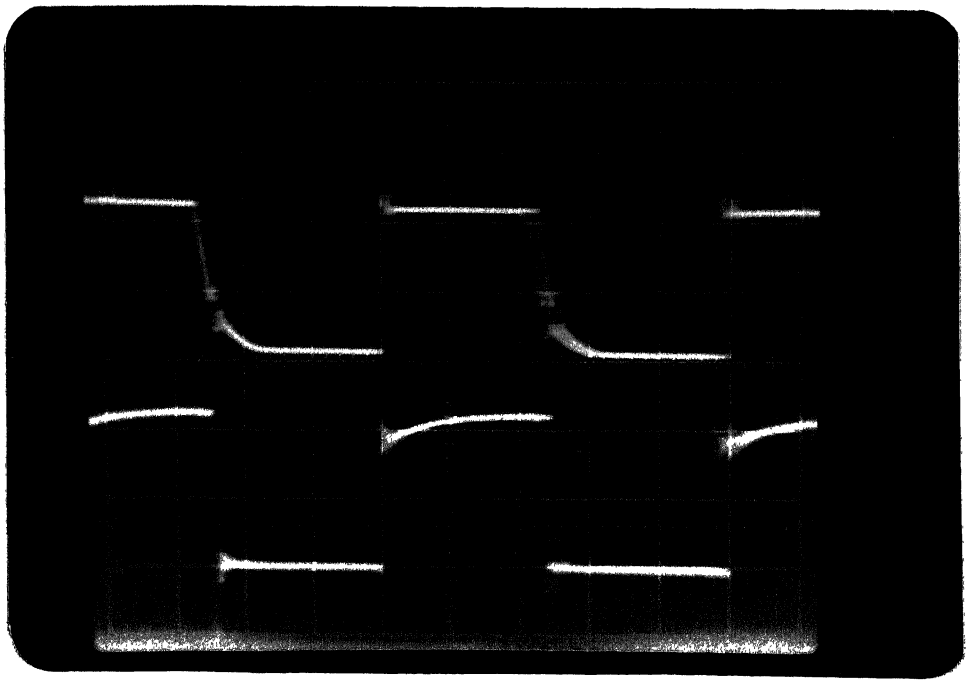


FIGURE E4 : Generation of clock pulse for counter 2 for addressing main ROM_3

(i) Buffered clock pulse

2 V/div, 2 μS/div

(ii) Pulses generated by PLL

2 V/div, 2μS/div

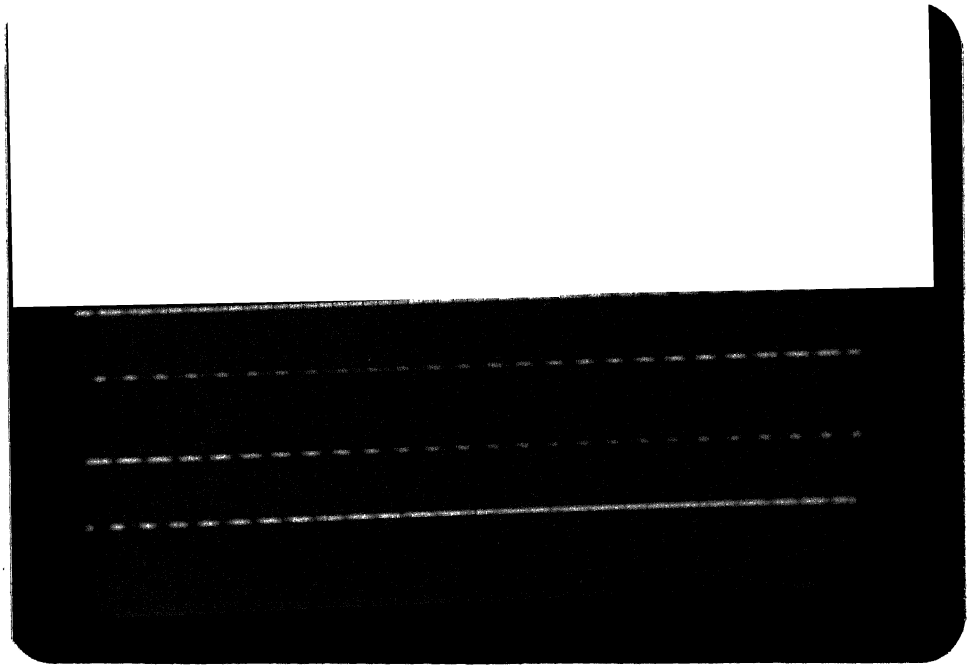


FIGURE E5 : PWM pulses for all the three phases (I_d = 3.6 A)
5 V/div, 2 mS/div.

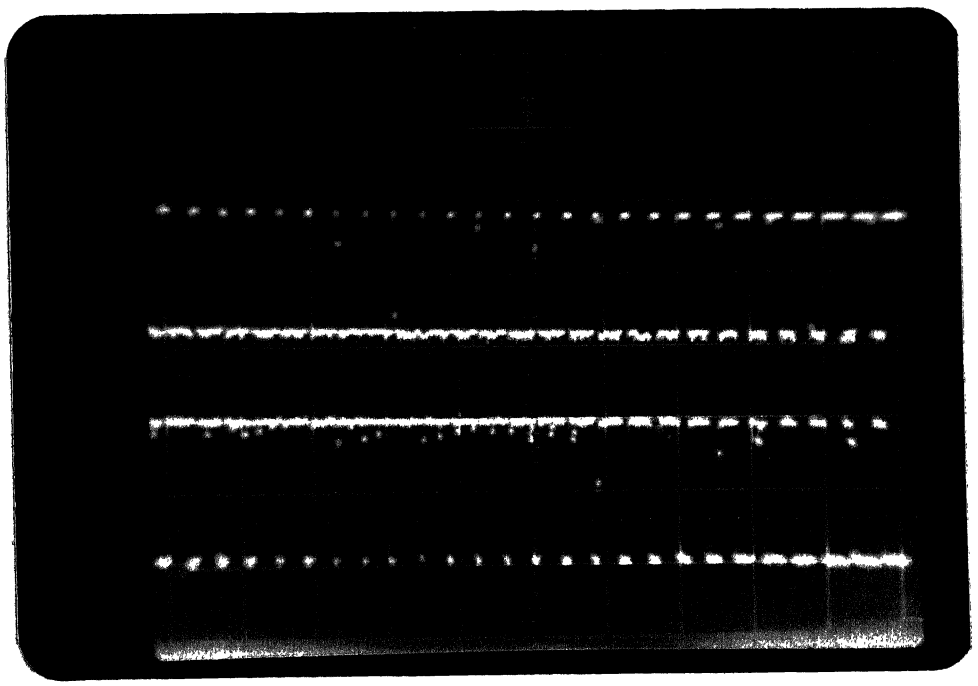


FIGURE E6 : PWM pulses for two switches of same leg
2 V/div, 1 mS/div.

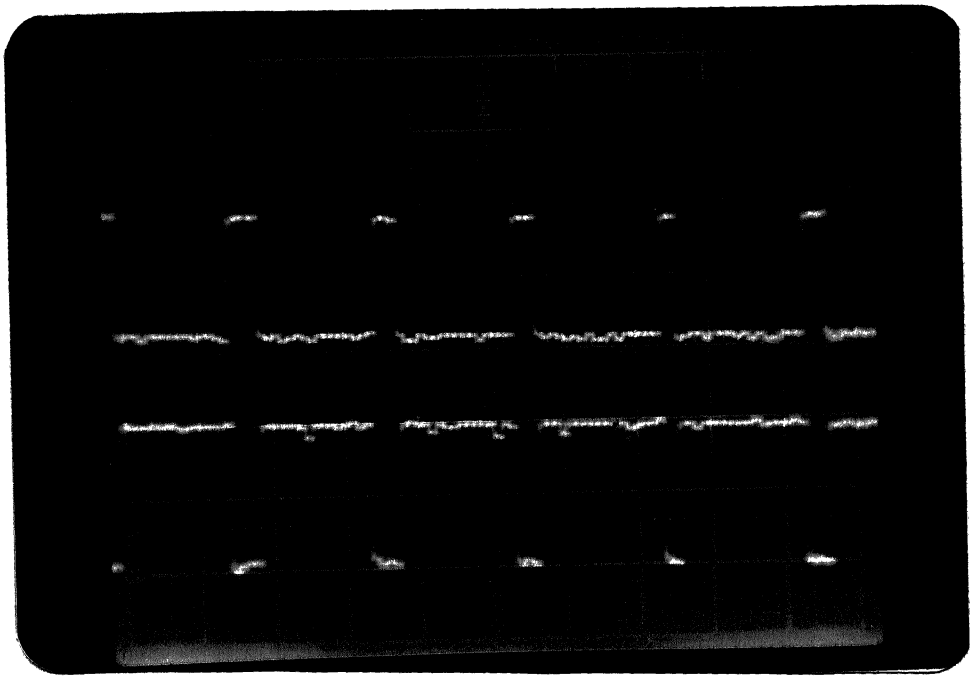


FIGURE E7 : Expanded (magnification = 5) view of FIGURE E6.

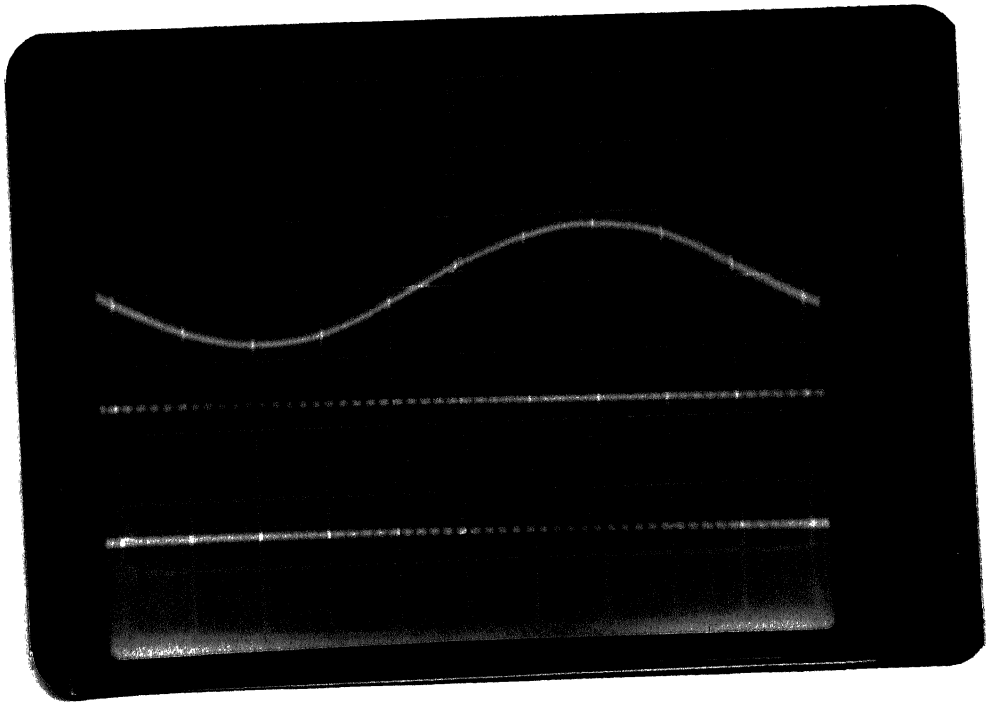


FIGURE E8 : PWM pulses for phase 'a' (I_d = 0)

(i) Reduced source voltage (phase 'a')
50 mV/div, 2 mS/div

(ii) PWM pulses for phase 'a'
2 V/div, 2 mS/div.

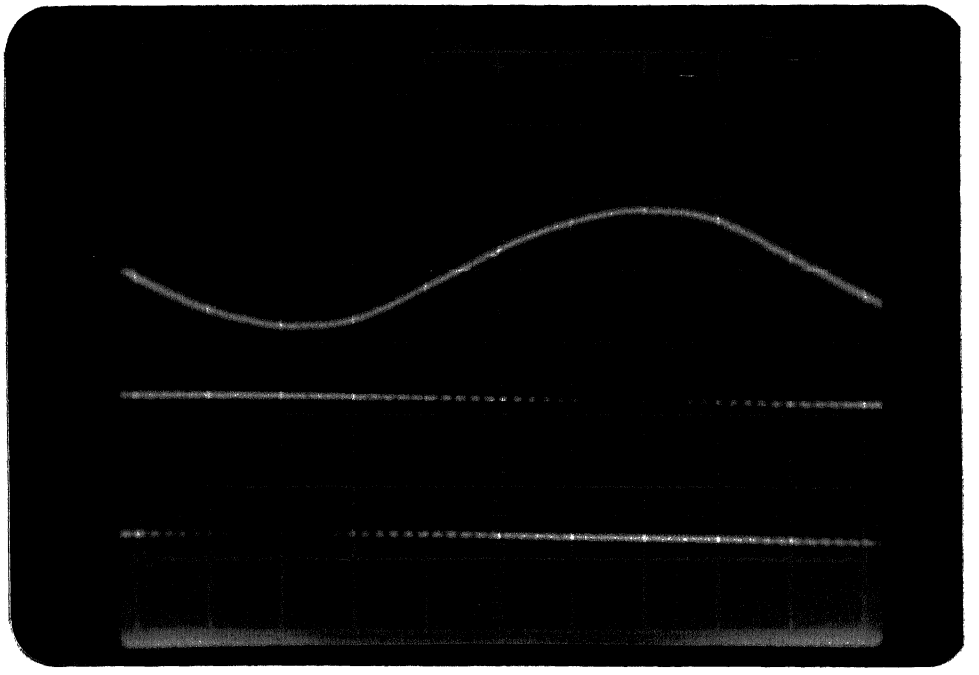


FIGURE E9 : PWM pulses for phase 'b' (I_d = -10 A)

(i) Reduced supply voltage (phase 'a')

50 mV/div, 2 mS/div

(ii) PWM pulses for phase 'b'

2 V/div, 2 mS/div.

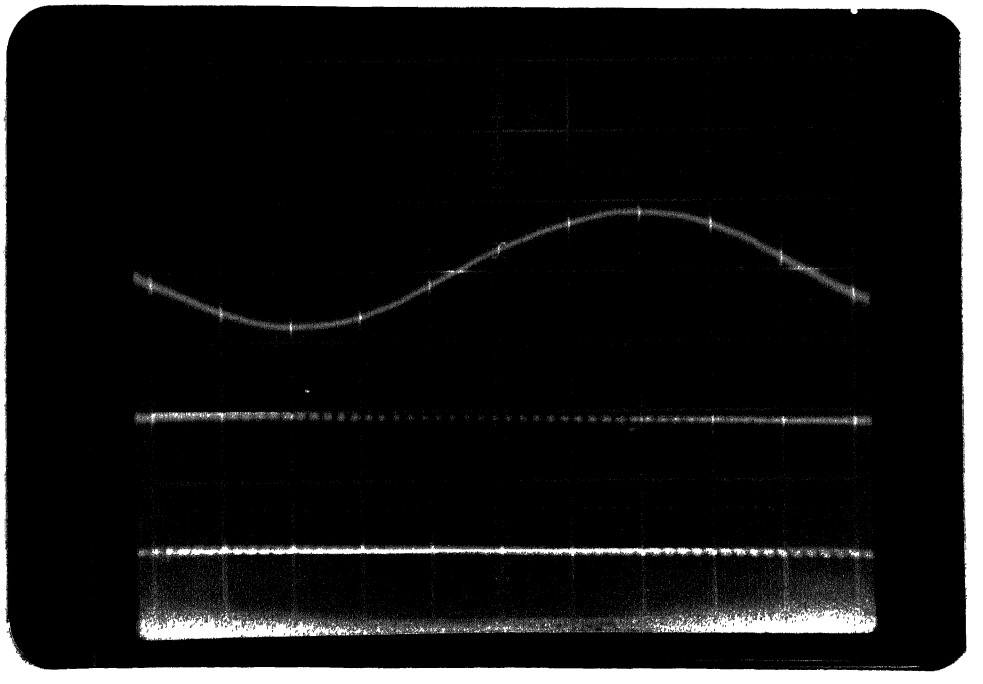


FIGURE E10 : PWM pulses for phase 'b' (I_d = 10 A)

(i) Reduced supply voltage (phase 'a')

50 mV/div, 2 mS/div

(ii) PWM pulses for phase 'b'

2 V/div, 2 mS/div..

CHAPTER 5

CONCLUSIONS

5.1 GENERAL

Bidirectional power converter can be employed as link between the DC and AC networks. The proposed control scheme takes into account the power variation on both the sides. If the power is more on one side and the load requirement on other side is higher, then the control scheme will sense the change of current on DC side and take appropriate action to restore the power balance by changing the modulation index and phase shift.

The control circuit is successfully tested for both the modes of bidirectional power converter operation namely rectification and inversion. The waveforms obtained experimentally confirm to those predicted analytically in the previous chapters.

The control scheme has an interesting feature of auto frequency adjustment. The frequency of state electricity board supply is prone to changes with load fluctuations. So any circuit based on fixed supply frequency will fall out of step whenever the frequency changes. This control circuit utilizes second order PLL (phase locked loop) which takes necessary action to change the frequency of pulse width modulated waves with that of source voltage. The circuit is tested at frequency band of 47 Hz - 53 Hz and is found to operate successfully. This band can be increased by changing R,C components of PLL.

The control circuit is employing dedicated hardware circuit for pulse width computation so the scheme is quite fast and any change is taken care of in the next cycle itself. By appropriately changing the sampling instant of I_d, the scheme may be operated at even faster speeds.

Most important aspect of the scheme is the unity power faster operation in both rectification and inversion mode. However, a look at Eqns.(3.6) and (3.7) shows the capability of the scheme to be used for even leading power factor.

The non-availability of appropriate size of ROMs and correct word size ADC has led to use over capacity ROMs which can be replaced by one of correct size to reduce storage space.

5.2 OTHER SCHEMES

The main object of the present work is to explore the capability of VSI to be used as a bidirectional converter. The derivations in Chapter 3 show the capability. Now any control scheme of conventional voltage source inverter can be modified easily to cater for the requirements of the bidirectional power converter.

An alternative to the existing control scheme can be one which does the on line computation of 'δ' and 'm_i' (phase shift, modulation index) and generates the necessary firing pattern. This will reduce the large ROM memory requirement. However, the computation time will slow down the speed of response of the scheme.

5.3 FUTURE EXTENSION OF WORK

Any control circuit is not complete without the associated power circuit.

As explained in Chapter 2 power MOSFETs are the ideal choice for medium power, high frequency converters. The pulse width modulation requires higher switching speeds which can be met by MOSFETs more effectively. Also MOSFETs offer built in antiparallel diodes which eliminates the need of external free wheeling diodes. Thus, simplifying the power circuit considerably. Low gate drive requirement is yet another advantage which simplifies the control circuit.

Power MOSFETs procurement was tried right from starting of project. However, due to non-availability of appropriate rating MOSFETs the control scheme could not be tested on the power circuit. However, the firing pulses for all the 6 switches are obtained and verified for different load conditions.

The MOSFET bidirectional power converter circuit, for which protection and other details are given in the report, will be next step in establishing the bidirectional capability of the voltage source inverter experimentally.

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